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JUN 77 R W BURROWS, R A HOLTZ F33615-74-C-1107
UNCLASSIFIED MCR-74-164 AFAL-TR-77-62 NL

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AFAL-TR-77-62

MICRON RELIABILITY ANALYSES

Martin Marietta Corporation
P.O. Box 179
Denver, Colorado 80201

June 1977

TECHNICAL REPORT AFAL-TR-77-62

Final Report for Period April 1974—April 1977

Approved for public release; distribution unlimited

AIR FORCE AVIONICS LABORATORY
AIR FORCE WRIGHT AERONAUTICAL LABORATORIES
AIR FORCE SYSTEMS COMMAND
WRIGHT-PATTERSON AIR FORCE BASE, OHIO 45433

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER: AFAL-TR-77-62	2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE (and Subtitle): MICRON Reliability Analyses	5. TYPE OF REPORT & PERIOD COVERED: Final Technical Report, April 1974 - April 1977
6. PERFORMING ORG. REPORT NUMBER: MCR-74-164	
7. AUTHOR(s): Richard W. Burrows; Ray A. Holtz	8. CONTRACT OR GRANT NUMBER(s): F33615-74-C-1107
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Martin Marietta Corporation, P. O. Box 179, Denver, Colorado 80201	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 666A-03-23
11. CONTROLLING OFFICE NAME AND ADDRESS: Air Force Avionics Laboratory, Air Force Wright Aeronautical Laboratories, AFSC, Wright Patterson AFB, OH 45433	12. REPORT DATE: June 1977
	13. NUMBER OF PAGES: 166
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): 167p.	15. SECURITY CLASS. (of this report): Unclassified
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Micro Navigator (MICRON); Reliability.

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The report summarizes the work accomplished by Martin Marietta Corporation in assisting Rockwell International, Autonetics Group, in the area of Reliability on Project No. ADP 666A, the development of a Micro Navigator (MICRON). This reliability assistance was provided from April 1974 through April 1977.

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PREFACE

This MICRON Reliability Analysis Program Final Technical Report has been prepared by Martin Marietta Corporation in response to a requirement of CDRL Item No. A009, on Contract F33615-74-R-1107, and Amendment F33615-74-C-1107, with Wright Patterson Air Force Base, AFAL.

During the three-year period of performance, Martin Marietta Corporation provided reliability assistance to the AFAL on the development of the Micro Navigator (MICRON). Program personnel were:

R. W. Burrows ..... Program Manager

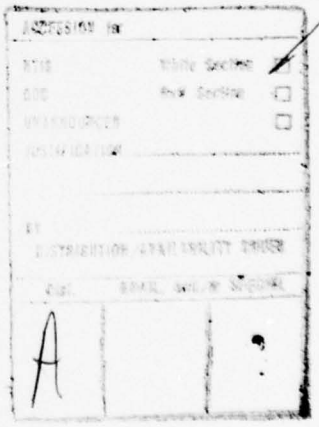
R. A. Holtz ..... Technical Director

J. C. DuBuisson ..... Reliability Assessments

J. R. Beall ..... Beam Lead Industry Survey

L. E. Bergquist ..... Vacuum Problems

The AFAL Technical Monitor was Capt. George Radic during 1974 and Mr. David Pleva for the remainder of the Program (1975-1977).



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SUMMARY

The purpose of the program was to assist the Avionics Laboratory in the achievement of high reliability and low cost-of-ownership for the Micro Navigator (MICRON), Project No. ADP 666A.

An experienced Martin Marietta reliability engineer was relocated at the Autonetics facility and remained there for most of the three-year period of performance; April 1974 through April 1977. During this period, the reliability tasks completed included program familiarization and preparation of reliability guidelines, the development of a Reliability Program Plan and a Reliability Test Plan, the development of a MICRON reliability model, iterative reliability predictions using MIL-HDBK-217B, the development and maintenance of a MICRON Parts List, participation in cost-of-ownership trade studies and design reviews, the development and initiation of a failure reporting system, monitoring of GIDEP ALERTS, the completion of many reliability assessment studies and industry surveys, and assistance in many discrete areas.

At the completion of this contract, a very strong conviction exists that MICRON will achieve its future reliability expectations.

SECTION I

INTRODUCTION

1.1 Objective. The purpose of the MICRON Reliability Analysis Program was for Martin Marietta Corporation (MMC) to assist the Air Force Avionics Laboratory to achieve a MICRON Inertial Navigation System that would exhibit a high reliability and provide a significantly reduced cost-of-ownership.

The approach used by MMC to help attain the specified program goals included, but was not limited to, preparing a reliability program plan and reliability test plan, performing independent reliability analyses and assessments, preparing design guidelines, performing trade off studies, developing reliability models, supplying data in accordance with the CDRL, and monitoring testing. These efforts are discussed in detail as separate tasks in the following paragraphs.

SECTION II

TECHNICAL DISCUSSION OF APPROACH USED

The first step to accomplish the objective was to establish an MMC Reliability Engineer in residence at the Rockwell Autonetics plant in Anaheim, California. This move placed MMC in a position to obtain immediate firsthand information concerning technical details of the program and gave our on-site reliability engineer a better opportunity to make technical contributions to the MICRON design and testing. To accomplish the detailed objectives of the program, MMC performed certain specified tasks as follows.

2.1 Task 1 - Program Familiarization and Development of Guidelines. The statement-of-work called for MMC to expend approximately two months to become thoroughly familiar with the MICRON program. Emphasis was to be placed on understanding the cost-of-ownership aspects of the program. Based upon the learning process, and prior experience, MMC was to develop reliability design guidelines. These guidelines would include general engineering practices which would be necessary to achieve MICRON's reliability goal.

2.1.1 Familiarization Strategy. The MICRON program familiarization task was accomplished by the relocation of Ray Holtz (MMC) to the Autonetics facility on June 10, 1974, by reviewing MICRON N57A documents, by interchanging data with Autonetics personnel, by initiation and assembly of a library of applicable technology, by three briefing trips to Autonetics by R. W. Burrows (MMC), and by MMC participation in the MICRON design review of July 23, 1974.

MMC familiarization strategy included the development of a good working rapport with Autonetics personnel and, accordingly, any and all requests from Autonetics for data or assistance was expedited in the most responsive manner possible. During this familiarization period, MMC supplied Autonetics the material as listed below.

(a) Information on package sealing techniques.

(b) Information on MMC's hybrid facility.

(c) Information on the accuracy of reliability predictions.

(d) Information on temperature cycling.

(e) Information on silicone curing.

(f) Arrangements were made to have a quart sample of Uralane conformal coating shipped to Autonetics.

(g) Four volumes of an MMC Long-Life Assurance Study was provided for Autonetics.

Familiarization discussions were held with MICRON reliability and electronics design personnel regarding the electronic parts derating policy and the performance of worst-case stress analysis on the MICRON electronic circuits and parts. Technical discussions were also held with MICRON reliability, systems engineering and test personnel, and with the MICRON electronic parts engineer concerning electronic parts procurement, traceability, and storage of the parts. These discussions revealed that the parts derating policy being used was in conformance with good derating practices and sufficient to achieve reliable operation of the electronics from a derating standpoint. Their worst-case analysis studies were documented and reviewed by appropriate people and design action taken when deemed necessary. MICRON procurement, traceability, and storage of electronic parts was satisfactory for this program and nothing was found in this area which would cause degradation of the electronic parts.

During this period of initial familiarization with MICRON, it was concluded that the reliability of MICRON was strongly dependent on the understanding and the utilization of the rapidly developing technology on hybrid microelectronics. Accordingly, a library of applicable technology was developed and is summarized below:

Subject	Applicable Papers and Reports
Cost-of-Ownership	6
Hybrid Reliability	18
Hybrid Coatings	21
Beam Leads	2
Wire Bonds	3
Hybrid Processes	1
Liquid Cooling	3
Thick and Thin Film Resistors	4

Subject	Applicable Papers and Reports
Screening	7
Reliability Demonstration Testing	2
Viking Parts Problems	4

These documents provided valuable source data on failure mechanisms, guidelines, and reliability to both MMC and Autonetics personnel.

2.1.2 Design Guidelines. Reliability design guidelines judged to be applicable to the MICRON program, including general engineering practices necessary to achieve MICRON's reliability goal, were prepared by MMC. These guidelines were based on MMC's learning process and prior experience and expertise in the field of reliability, design, build, and testing of electronic hardware.

Many of the guidelines selected for the MICRON program were among the 650 guidelines established by MMC and NASA-JSC for use in the Space Shuttle and other NASA programs. Only guidelines compatible with aircraft environment and reduced cost-of-ownership were selected from this group. Additional guidelines were also developed to provide for new situations unique to the MICRON program.

The guidelines were completed and published August 15, 1974. At a later meeting, with reliability and other MICRON engineering personnel, copies were provided for Autonetics' use on the program. Considerable use was made of the guidelines, particularly in the area of electronic parts derating. A copy of the published guidelines is shown in Appendix A.

2.2 Task 2 - Reliability Program Plan and Reliability Test Plan. In this task, the statement-of-work called for MMC to develop a MICRON reliability program plan and reliability test plan using MIL-STD-756, -781, and -785 as guides. Deviations to the above standards were to be recommended, where appropriate, and when such deviation could be justified based upon MMC prior experience.

2.2.1 Early Reliability Plan. In accordance with the MMC contract schedule, an early Reliability Program Plan was developed by MMC and published in September 1974, as MCR-74-356. This plan constituted a planning and control document for implementation of reliability tasks by Autonetics. The document was written so it would be consistent with the

number of engineering and development systems as determined for the initial Phase 2B program described by AFAL statement-of-work for the preproduction and production phase of the MICRON program.

At the early date that this program plan was written, which was prior to a firm MICRON preproduction and production contract, the actual data needed to make many of the figures and tables complete was not available. Also, at this time MIL-HDBK-217B was not officially published by the Department of Defense, thus the mathematical model shown in the program plan was not the one actually used for reliability predictions. The new MIL-HDBK-217B, Notice 1, mathematical model was the one actually used for all of the MICRON program reliability assessments accomplished. If at a future date, Autonetics is required to prepare a Reliability Program Plan, the above referenced plan could be used as a guide.

2.2.2 Reliability Demonstration Test Plan. In accordance with the MMC contract schedule, a Reliability Demonstration Plan was prepared by MMC and submitted in September 1974. This plan was based on MIL-HDBK-781B. This plan was formulated and submitted after an extensive dialogue between personnel at WPAFB, RADC and industry. The purpose of these discussions was to resolve several issues pertaining to certain inadequencies in MIL-STD-781B; "Reliability Tests: Exponential Distribution". These issues are discussed below and it will be seen that the forthcoming revision of MIL-STD-781B (Revision C) will eliminate the concerns described herein. Revision C was worked on throughout 1976 and early 1977, and should be officially released in 1977. The revision work is being accomplished by D. D. Perkins, Naval Electronic Systems Command; and AIA Coordinator, J. W. Engdahl, Honeywell, Inc., 6000 2nd street, N.E., Hopkins, MN 55343.

MIL-STD-781C is a complete revision of MIL-STD-781B and makes extensive use of appendices. The appendices expand and clarify various sections of the standard and will aid both procuring activity and producer in the application of this standard.

The issues addressed in the formulation of our plan and the key issues, which have been addressed by government and industry during the development of Revision C, are summarized.

(a) Accuracy of the Environmental Simulation

Recent studies by RADC, Grumman, Col. Ben Swett, and others, have concluded that a prime reason for lower field reliability than that demonstrated by MIL-STD-781 testing, is the failure of the 781 test to realistically duplicate the use environment. Accordingly, MIL-STD-781C has discarded the 10 arbitrary test levels and has

substituted a basic requirement to synthesize a realistic environmental test profile based on an accurate analysis of the use environment. The new document provides considerable guidance on this point and includes sample environmental test profiles.

(b) Sinewave vs Random Vibration

Our plan abolished the 2.2g sinewave specified in 781B as unrealistic. This proved to be correct as the new MIL-STD-781C will specify random vibration with the level depending on zonal location of the equipment within the aircraft. A level of $0.01g^2/Hz$ appears applicable to MICRON.

(c) Relevant Failures

RADC and Grumman developed an improved set of definitions for determining which 781 test failures are chargeable against the MTBF as relevant failures. Accordingly, MIL-STD-781C will contain improved definitions of relevant and non-relevant failures.

(d) Combined Environmental Test Conditions

Another major change in MIL-STD-781 is the use of combined environmental test conditions (temperatures, vibration and moisture) based on the actual mission profile environments encountered during the equipment's useful life.

The moisture (humidity) need not be held constant, and the desired result can be obtained by periodically injecting water vapor into the test chamber.

Altitude has not been included with combined environments because in a majority of cases it does not contribute significantly to reliability problems. However, in those cases where it could, provision is made for the contract to incorporate it.

(e) The new 781C encourages the use of reliability growth testing prior to final reliability qualification testing. This concept was proposed in our plan and agreed to in principal by Autonetics, but constraints on program funding prevented its adoption. However, Autonetics

is subjecting their hybrids to environmental exposures which partially accomplishes the intent of this testing in a qualitative rather than quantitative way.

(f) The definitions of the mean-time-between-failures (MTBF) requirements have been changed to clarify the use of θ_0 and θ_1. θ_1, the "low-limit" MTBF, is the contractually required MTBF and θ_0 is the "design" MTBF. The ratio of θ_0 to θ_1 is now defined as the "design" ratio. Since the design ratio takes the place of the discrimination ratio, it also determines what test plan can be effectively utilized. The new definitions enable the low-limit MTBF to be held constant (which should be the case since that value is the lower limit of the MTBF required in the field) when choosing a test plan. Previously, under -781B, the "minimum acceptable" MTBF changed with the test plan making the concept of a minimum acceptable (or a lower limit) MTBF ineffective. It could assume any value from 2/3 to 1/5 of the specified MTBF (θ_0), depending on the test plan selected.

The above discussion is presented to assist WPAFB and Autonetics MICRON personnel, since Autonetics may, at a future date, be required to prepare the final Reliability Demonstration Plan. In this event, it will be important to use MIL-STD-781C, rather than the "B" version. In addition, WPAFB may have to supply, or make available, the detailed mission environmental data to enable Autonetics to synthesize a test which accurately simulates the mission environment, rather than the approach of using one of the test levels now prescribed in 781B. This approach is superceded by the new approach delineated in 781C.

2.3 Task 3 - Reliability Assessment. The statement-of-work for this task called for MMC to participate in the Phase 2A and 2B MICRON system design activity by developing a MICRON reliability model and by performing independent reliability assessments. Additionally, MMC was to recommend design changes, when necessary, to achieve MICRON's reliability goals.

2.3.1 Assessment Models. Initial independent reliability assessments were begun by MMC in July 1974. These assessments were generated by using a baseline parts list. This list was being updated almost weekly during the first few months of MMC participation in the MICRON program. In addition to the parts list changes, MIL-HDBK-217B was also in a state of revision.

In September 1974, MMC received the finalized version of MIL-HDBK-217B and the Notice 1 changes to it in September of 1976. During the period between September 1974 and September 1976, many MICRON reliability assessments were completed and published in the MMC monthly and quarterly reports. These reliability assessments represented various MICRON configurations and several reliability models, depending upon the state of revision of MIL-HDBK-217B.

The latest reliability assessment models being used on the MICRON program are from MIL-HDBK-217B, Notice 1, as shown in Table 1.

With the introduction of MIL-HDBK-217B as the methods and models to use for reliability assessments, it was realized that this method of prediction would benefit by the development of a standard format to use for analyzing and documenting the various mathematical steps involved. With this in mind, MMC, with assistance from Autonetics reliability, developed various formats to use in making such reliability assessments. These formats are shown in Appendix B, Figures 1 through 15. These formats have been used continuously, not only by MMC, but also by Autonetics' reliability. The availability of these formats has saved many hours of time in making the multitude of trade offs and assessments needed to support the MICRON program. They have also provided excellent documentation which can be referred to and understood at any time.

2.3.2 Assessments. Appendix C summarizes the last MICRON reliability assessment completed by MMC and Autonetics prior to closing the MMC office at Anaheim. Two assessments are shown. The 1190 hours MTBF represents an update of the previous published assessment for the MICRON production model. The 175-hour MTBF is the first assessment for the Engineering Prototype Model (EPM). This 175-hour MTBF for the EPM is considered representative of the early prototype MICRON system reliability. It is perhaps even a little higher than expected, based on the starting points usually identified with growth curve projection. It is common for the early development hardware to exhibit about 10 percent of the mature hardware reliability, with hardware maturity occurring at between 3000 and 10,000 hours of MIL-STD-781B testing.

The production configuration represented by the above number assumed the substitution of the getter gyro for the vac-ion pump gyro which is used in the prototype configuration. Also, the production configuration uses the DMAC MOS device which replaces approximately 60 discrete ICs in the DPU I/O module, and the substitution of ROMs for PROMs in the DPU memory module. One of the greatest differences between the production and prototype systems is the quality level of the solid-state devices (i.e., ICs, transistors, and diodes). For example, in the production configuration most of the ICs will be of the upper quality levels (i.e.,

TABLE 1

Reliability Assessment Models

Device or Part Type	MIL-HDBK-217B - Notice 1	
	Paragraph No.	Page No.
Hybrids	2.1.7	2.1.7-1/-12
Integrated Circuits		
Monolithic Bipolar and MOS Digital SSI/MSI Devices (less than 100 gates)	2.1.1	2.1.1-1
Monolithic Bipolar and MOS Linear Devices	2.1.2	2.1.2-1
Monolithic Bipolar and MOS Digital LSI Devices (equal to or greater than 100 gates and equal to or less than 1300 gates)	2.1.3	2.1.3-1
Monolithic MOS and Bipolar Memories	2.1.4	2.1.4-1
Discrete Semiconductors		
Transistors	2.2	2.2-1
Diodes - selected by group number	2.2.4/8	2.2.4-1/2.2.8-1
Discrete Resistors		
Resistors (fixed)	2.5	2.5-2
Resistors (variable)	2.5.5	2.5.5-1
Discrete Capacitors - Selected for type	2.6	2.6-1/2.6.9-4
Inductive Devices - Selected for type	2.7	2.7-1/2.7-14
Relays	2.9	2.9-1/2.9-8
Switches - Selected for type	2.10	2.10-1/-6
Connectors - Selected for type	2.11	2.11-1/-12
Wire & Printed Wiring Boards - Selected for type	2.12	2.12-1/-5
Miscellaneous Parts - Selected for type	2.13	2.13-1/-2

π_Q multiplying factors of 2 and 5). In the prototype mode, the ICs are of the best commercial grade level (i.e., π_Q multiplying factor of 150). In most cases, the prototype solid-state devices have been adjusted upward to a π_Q of 50. This upward adjustment reflects the extra screening and/or testing received at the module or system level.

From this difference in multiplying factors between the 2 and 5 of the production system and the 50 of the EPM system, it can be seen that the quality level of electronic parts has a very significant impact on the level of assessed reliability. Figure 1 graphically depicts the tremendous difference in assessed reliability due to the quality factor multiplier. The MICRON processor memory is used for this example because it represents approximately 54% of the total EPM Data Processor Unit (DPU) failure rate and the DPU represents 64% of the total MICRON EPM system failure rate. Also, the integrated circuits of the processor memory represent 99.4% of the total processor memory failure rate. The total processor memory is assessed at 1960 failures per 10^6 hours.

With the above background information, an analysis of Figure 1 data clearly shows that a decrease in part quality of discrete integrated circuits from MIL-M-38510, Class "B", to a MIL-STD-883, Class "C", causes a 97.8% decrease in MTBF per MIL-HDBK-217B.

To further facilitate examination of the MICRON system details by Autonetics and MMC, an analysis was performed by MMC which compares the failure rate by component mix and is depicted in Table 2.

2.3.3 MICRON Parts List. All good reliability assessments must begin with a good parts list. Thus, early in the MICRON program, MMC developed a parts list format specifically for the MICRON program. This parts list format recognized the systems subassemblies and ceramic printed circuits (CPCs) down to the discrete parts/chip level. These parts lists were so complete and easy to use that it soon became very much in demand. Autonetics MICRON engineers requested copies and continuously used these parts lists, thus it became important for MMC to undertake the task of updating this list as often as practical.

The parts count summary is shown in Table 3 and gives the part totals by part category for the various MICRON subassemblies. Table 4 is a further breakdown of the parts to show whether they are beam lead, fly wire chip, or discrete parts. Appendix D shows a sample of the format used for the parts list.

2.3.4 Technical Studies. MMC developed a number of technical studies which were beneficial to the MICRON program. Some of these studies were related to significant design problems and some were related to potential design problems.

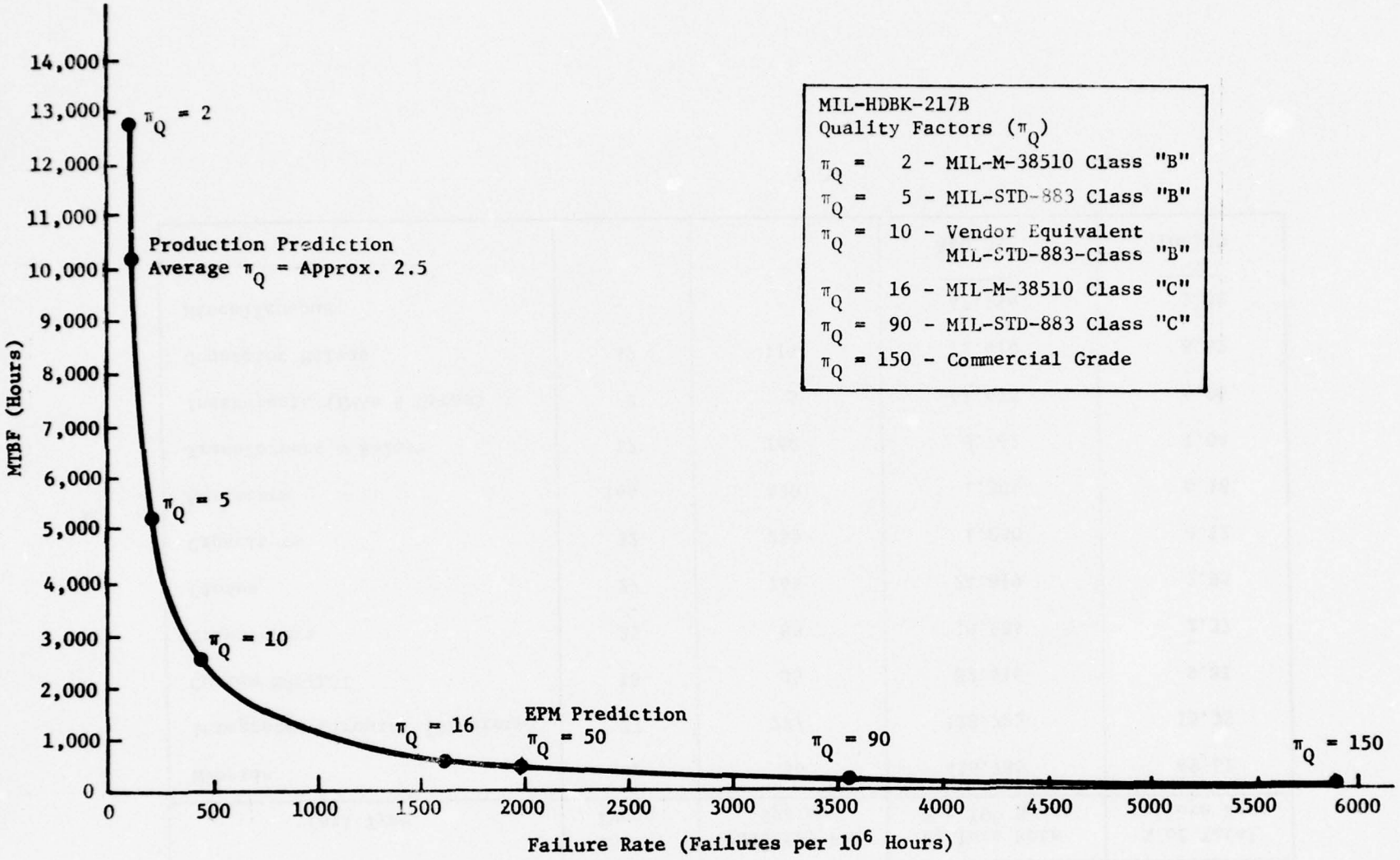

Figure 1. MICRON DPU Processor Memory - Integrated Circuit Reliability Change vs Quality Factor (π_Q) Change

TABLE 2

Failure Rate By Component Mix

Part Type	No. of Types	Quantity Per System	Failure Rate Per 10^6 Hours	% of Total Failure Rate
Hybrids	32	66	416.785	49.62
Integrated Circuits (Discrete)	77	277	128.782	15.33
Custom MOS/LSI	18	35	82.416	9.81
Transisters	25	83	19.934	2.37
Diodes	27	143	24.819	2.95
Capacitors	32	255	1.030	0.12
Resistors	144	430	1.301	0.16
Transformers & Relays	17	162	8.742	1.04
Instruments (EMAs & Gyros)	2	5	41.675	4.96
Connector Halves	39	116	72.410	8.62
Miscellaneous	-	-	42.156	5.02
			840.05	100.00

TABLE 3

Phase 2B MICRON Prototype Model (EPM) INU Parts Count
Revision 2 for N73 (Rotated System)

ITEM	SEU 1	SEU 2	SEU 3	SEU 4	DPU	CNVTR	DATERM	IAU	SMU	PSU	MHU	TOTAL
Ceramic Capacitors	116	116	75	37	49	99	73	136	9	51	8	769
Tantalum Capacitors	0	0	4	0	4	9	2	67	4	33	0	123
Diodes	8	8	15	11	2	37	6	169	21	95	21	393
ICs	62	62	68	34	251	55	163	69	12	18	2	796
Discrete Resistors	32	32	4	13	70	70	40	72	47	153	27	560
Miscellaneous Parts	14	14	16	6	9	16	11	129	16	18	57	306
Transistors	0	0	8	15	0	4	42	65	22	48	7	211
Subtotal	232	232	190	116	385	290	337	707	131	416	122	3158
Screen Resistors	323	323	142	71	0	171	100	435	35	0	0	1600
GRAND TOTAL	555	555	332	187	385	461	437	1142	166	416	122	4758

TABLE 4

MICRON INU Parts Usage Summary - EPM

Part Category	Beam Lead	Fly-Wire Chip	Discrete	Total
Integrated Circuits (Total)	67	317	412	796
Digital	52	86	319	457
Linear	15	168	28	211
MOS/SSI	-	58	3	61
MOS/LSI	-	5	62	67
Transistors	65	63	83	211
Diodes	160	90	143	393
Capacitors (Total)	-	649	255	904
Ceramic	-	578	187	765
Tantalum	-	71	68	139
Resistors	-	141	430	571
Connector (Halves)	-	-	116	116
Miscellaneous	-	-	162	162
Sub-Total	292	1260	1601	3153
Screened Resistors	-	-	-	1600
GRAND TOTAL	-	-	-	4753
Total Number Hybrids				66

This study data was taken into consideration by MICRON design personnel in determining a problem solution or prevention, whichever the case might have been. Table 5 shows a list of the technical studies which were supplied by MMC to help insure a reliable INS.

The information contained in some of these studies, not only is appropriate to the MICRON program, but would also be of particular interest and value to other AFAL electronic hardware programs. For example, the "Beam Lead Technology Review", shown in Appendix E, details the status as of July 1975 and projects the future for beam lead semiconductor devices, identifies problems and trade off considerations for feasibility assessment and presents guidelines. Autonetics conducted a parallel beam lead study with their information published in Rockwell Report No. 75-244-065, MICRON-091.

The latest usage data for the MICRON hardware shows a total of 292 beam lead devices being used. They are divided as follows: 67 integrated circuits (ICs), which is 8.4 percent of the MICRON total ICs; 65 beam lead transistors, which represents 30.8 percent of the MICRON transistors; and 160 beam lead diodes, which represents 40.7 percent of the total diodes used in the MICRON system.

In June of 1974, Autonetics was pursuing the development of a beam lead carrier device for integrated circuits on an AFAL funded program. This carrier device, when satisfactorily completed, would provide for more satisfactory testing of the beam lead ICs and would enable burn-in and screening prior to installation into MICRON hardware. Later, the AFAL task was deleted and, at the present time, Rockwell funds are being used to complete this development.

The wet slug tantalum capacitor (WST) study, presented in Appendix F, is another study that may be useful in other AFAL programs. There was an application in the MICRON power supply where the WST had been tentatively considered. The study was performed by MMC to emphasize the importance of eliminating WST capacitors from any MICRON prospective designs. As a result of this study, and MMC/AN reliability efforts, more physical space was made available in the design to accommodate the more reliable solid tantalum type capacitors.

Another study example is the "Cost-of-Ownership Trade Off Study of Temperature Cycling Acceptance Testing of MICRON". This study; 1) establishes the most cost-effective number of temperature cycles to use for MICRON during acceptance testing, 2) estimates the overall cost savings to the government, and 3) gives a comparative analysis of monitoring first and last temperature cycles versus continuous test monitoring. This study, presented as Appendix G, concludes that eight temperature cycles

TABLE 5

Technical Studies Performed by MMC for MICRON Program

Subject	Brief Description	Published in MCR-74-164		Design Effect
		Issue No.	Date	
Coatings for Hybrid Microcircuit Protection	Details of MMC experience, results of a GSFC contract study by MMC, and a summary of industry survey concerning the use of coatings for hybrid microcircuits and the problems encountered.	3	July 1974	Used sealed metal lids over hybrids thus eliminating need for any coating.
Parts Commonality Study	MMC performed an analysis of electronic parts usage. Developed a list of high usage parts from which to choose substituting for low usage parts.	9	Jan. 1975	This list was used by electronics design engineer and parts engineer to obtain candidate parts.
Beam Lead Technology	A beam lead technology review conducted by MMC. It summarizes the current status and the projected future for beam lead semiconductor devices.	15	July 1975	Reduced somewhat the number of beam lead candidates for MICRON use.
Cost Trade Off Study	MMC developed reliability/cost guidelines to obtain a quick evaluation of the cost benefits of a proposed reliability improvement change.	15	July 1975	Determines which reliability improvement change should be rejected and a lower cost solution sought.

TABLE 5 (CONTINUED)

Technical Studies Performed by MMC for MICRON Program

Subject	Brief Description	Published in MCR-74-164		Design Effect
		Issue No.	Date	
Wet Slug Tantalum Capacitor Study	A review of MMC data for MICRON electronic designers concerning the silver migration problem in wet slug tantalum capacitors.	15	July 1975	Wet slug tantalum capacitors were designed out of the power supply circuit.
Cost-of-Ownership Trade Off Study	MMC performed this study to establish the most cost-effective number of temperature cycles for preliminary debugging of MICRON electronics to eliminate a major portion of infant mortality failures in the production hardware. It also concludes that it is cost-effective to monitor only two (first and last) cycles of the temperature test rather than all the cycles, and estimates the overall cost savings to the government of a stringent acceptance test program.	15	July 1975	Provides the MICRON program with data for design of a debugging test on production hardware prior to acceptance testing. Also, proposes a cost-effective method of monitoring these tests.
Compendium of Data Relevant to the Update of the Reliability Demonstration Test Plan	This study performed by MMC contains comments and recommendations to update MCR-74-357, MICRON Reliability Demonstration Plan. The comments were offered by WPAFB, RADC, and Autonetics. The recommendations are the result of major conclusions drawn by MMC from the referenced RADC/Grumman report and WPAFB/General Electric report.	18	Oct. 1975	Provides Autonetics with data pertinent to developing an effective reliability demonstration test plan for the MICRON production hardware.

TABLE 5 (CONTINUED)

Technical Studies Performed by MMC for MICRON Program

Subject	Brief Description	Published in MCR-74-164		Design Effect
		Issue No.	Date	
Demonstrated Growth Curve for N57A-1/-2	Depicts a demonstrated growth curve by N57A-1 and N57A-2. The data for the calculation of the curve was obtained by reviewing in detail the equipment log books for each of the two units and determining the applicable failures and running time.	18	Oct. 1975	Provides assistance in determining a growth projection for MICRON.
Reliability Investigation of Ion Pump Sure-Start Filament	Documents the results of an investigation conducted by MMC/AN reliability concerning the electrical overstress condition existing in the sure-start filament of the vac-ion pump.	24	April 1976	Because the vac-ion pump is not in the production hardware but only in the engineering prototype hardware and due to the extremely short filament duty cycle, no design change was recommended. However, as a result of this investigation a small mechanical corrective design change was made in a new design to allow a complete through path for the filament ions to propagate into the interior chamber of the ion pump.

Technical Studies Performed by MMC for MICRON Program

Subject	Brief Description	Published in MCR-74-164		Design Effect
		Issue No.	Date	
Electromechanical Relay Study	Study was performed by MMC/AN reliability on electromechanical relays used in MICRON. Study had a twofold purpose. (1) Performed a reliability assessment on the relays using detailed application and stress derating data. (2) Conducted a trade off study to determine the reliability impact of substituting solid-state relays for electromechanical relays.	24	April 1976	(1) An assessed reliability improvement of 68 hours MTBF resulted from using the detailed application and stress derating data. (2) Substitution of solid-state relays for electromechanical relays appears worthy of consideration from the reliability viewpoint. It looks particularly advantageous for the fast warmup heater and d.c. switching applications.

conducted prior to formal reliability demonstration testing and then subsequently used as a 100% production acceptance test, will save the government upwards of one million dollars for the example case of 1000 production MICRONS.

2.3.5 Reliability Problems. Some reliability problems were identified to Autonetics, which did not necessitate a study by MMC, but which nevertheless needed to be evaluated by Autonetics. An example of one of these uncovered early in August of 1974 was a potential problem regarding the thermal environment of the Ni-Cad battery that was part of the MICRON system design at that time. The Ni-Cad battery was physically located in an area where the temperature at times exceeded the battery specifications. The Autonetics MICRON battery expert was advised of this problem, as was the MICRON electronics design supervisor, the thermal engineer, the systems and test supervisor, and the reliability engineer. After evaluating the details of the problem, they all agreed that it would need to be worked. Eventually, the problem went away because the battery now will be physically located external to the MICRON system.

MMC also provided assistance to Autonetics on known problems which Autonetics had already identified. An example of some problems where MMC provided assistance is as follows:

(a) Gyro Vacuum

An MMC vacuum expert (Mr. Lyle Bergquist) provided consultation early in March 1975 to Mr. H. L. Bump and Al Gross, and their MICRON team. The consultation concerned two vacuum problems which Autonetics was experiencing. The first discussion was in regard to the difficulty they were having in starting the vac-ion pump once it had been evacuated. The second discussion was twofold and concerned; 1) the achievement of a leak tightness in the "getter" gyro of 10^{-10} cm/second, and 2) outgassing processes that would effectively get rid of H_2O and N_2 molecules. Appendix H is a copy of a trip report memorandum written by Mr. Bergquist after his visit to Autonetics at Anaheim, California. Also included in this attachment is an information note from Al Gross at Autonetics. In the two years since MMC and Autonetics coordinated on this problem, Autonetics has continued development of both the vac-ion pump and "getter" gyros and implemented the necessary technical solutions.

(b) Triax Cables

A number of cases of triax cable problems began occurring in November 1976. These cables connect between the charge

amplifiers and the electrostatic gyro (ESG) plates. Such things as, connectors coming loose and wires breaking/ shorting at the connector, were occurring. The cables have a very small and quite stiff inner conductor with a layer of insulation covered by a shield, then another layer of insulation covered with a second shield, then a coating over the outer shield, and another stiffer coating over that. The cables are very short in length; approximately three to four inches, with a small connector on one end.

There are sixteen (16) of these cables and connectors in each EPM system. Each cable supplies a voltage to a plate of the gyro and sends information concerning the gyro back into the system. They are a very critical part of the gyro circuit.

MMC/AN reliablity initiated a meeting concerning this problem and action items were assigned to come up with a fix for this design. Several ideas were discussed. A triax cable with the stiff outer coating removed and a more secure way to fasten the connectors is being evaluated. Some additional new triax cable; more flexible than the old, has been received. This new cable will also be evaluated to determine the best solution for the problem.

The latest word that was available when MMC left Anaheim the last week of January 1977, was that the charge amplifier boards will plug directly into a connection with the ESG plates on the MICRON production systems, thereby eliminating entirely the triax cables and thus, the problem.

(c) Charge Amplifier MLBs

Another design problem, which surfaced during the integration testing at Autonetics test laboratory, was an apparent intermittent open or high resistance condition in the plated-through-holes on the charge amplifier MLBs.

All other MICRON MLBs used epoxy glass boards, but it was thought by electronics design that the charge amplifiers would need extra tolerance for capacitance effects. For this reason, teflon boards were used for the charge amplifiers only, to obtain this extra margin. Drilling for plated-through-holes is much more troublesome with the teflon material because it is difficult to always get the holes clean enough for good connections to be made with the metal layers when plating the holes.

As soon as it became apparent that this might be a problem, steps were taken by Autonetics to immediately remake the charge amplifier MLBs from epoxy glass boards. The epoxy glass boards drill clean and cause no intermittent connection problems with plated-through-holes. Also, it was found that the capacitance factor of the epoxy glass boards was no problem. All teflon charge amplifier MLBs have now been replaced with epoxy glass MLBs on the EPM systems.

2.3.6 Failure reporting. At a meeting between MMC and the MICRON Engineering Manager in July 1974, it was recommended by MMC that a failure reporting system be initiated on the Phase 2A hardware on which testing had already started. MMC became responsible for administering and fulfilling the role of reliability engineering for a MICRON program of failure reporting and failure analysis.

The reporting procedures and method of initiating failure reports were agreed upon at a later meeting attended by MMC and the appropriate MICRON engineers. This meeting was later followed by a program communication issued by the MICRON Engineering Manager (see Appendix I). A program bulletin was also issued by the MICRON Program Manager, Mr. J. A. Schwarz, for Phase 2A and updated in 1976 for Phase 2B EPM hardware as shown in Appendix J.

The failure reporting and failure analysis program was intentionally and selectively less formal than generally utilized for a development program. However, it did use the standard Autonetics "Form For Removal Reporting" (FRR shown in Figure 2) and their series procedure. The procedures were stripped down to the essential elements needed to allow MMC/AN reliability engineering to establish and analyze failure trends, hardware design problems, and permitted the assessing and recommending of corrective action.

This added task did not interfere with MMCs other duties; in fact, it provided for more effective reliability impact on the Phase 2A (N57A) and Phase 2B (EPM) hardware. It also prepared the appropriate MICRON engineers to become more knowledgeable in this failure reporting system so that even more data was obtained on Phase 2B EPM hardware and more contributions were made to make the EPM hardware more reliable.

As shown in Table 6, during the performance of the MMC contract, 150 failure reports were initiated, reviewed, and corrective action taken, when required. Thirty-three (33) of these reports were issued on the N57A-1/-2 program during Phase 2A. Much of the N57A testing had been completed prior to initiation of failure reporting. One hundred seventeen (117) failure reports were issued through January 1977 on EPM-1/-2 Phase 2B hardware.

00. IRIS CONTROL
DIV. | PROG. | CO

Autonetics Division
Rockwell International

01. REPORT 751454
02. INITIAL REPORT NO.
03. REPORTING ACTIVITY
04. LOCATION CODE

34. GO/SO NO.
35. PRR NO.
45. IMRO NO./CONTROL NO.

FRR FORM FOR REMOVAL REPORTING
(REPLACES FAILURE AND REPLACEMENT REPORT FORM)

47. CUST. REPORT NO. | A. | C. | 05. VEHICLE SER. NO.

06. EQUIP. TYPE, MODEL DSG, MOD. NO. | 07. EQUIP. SERIAL NO. | 08. REPORTABLE ITEM PART NO. | 09. REPORTABLE ITEM SERIAL NO.

10. REPORTABLE ITEM NOUN | 11. REP. ITEM MFG. | 12. ITEM REF. DSG. | 13. NEXT ASSEMBLY PART NO. | 14. NEXT ASSEMBLY SERIAL NO.

15. DATE OF EVENT MONTH DAY YEAR | 16. LOGISTICS INITIATED/IMRO ITEM 0 ☐ NO 1 ☐ YES | 20. REPLACEMENT PART NO. | 21. REPLACEMENT SERIAL NO.

OPER USAGE REPORTABLE ITEM ☐ ETM ☐ EST | 17. HOURS MINUTES SECONDS | CAL TIME (DAYS) | 19. ON-OFF OR CYC | 22. TROUBLE SHOOTING TIME (TENTHS) NO. OF MEN CLK. HRS. MAN HRS. | 24. REMOVE & REPLACE (TENTHS) CLK. HRS. MAN HRS.

27. REPAIR OR DISP. ACTION
1 ☐ REPAIRED IN PLACE
2 ☐ REPAIRED & RE-INSTALLED
3 ☐ ADJUSTED
4 ☐ HELD FOR ANALYSIS
5 ☐ CONDEMNED
6 ☐ HELD FOR REPAIR
7 ☐ DEPOT REPAIR
8 ☐ RETEST

29. TEST EQUIPMENT NUMBER
30. OPERATORS MANUAL
31. PARAGRAPH NUMBER

26. REASON FOR REPORT 0 ☐ NOT A FAILURE 1 ☐ FAILED ITEM
18. FAILURE CODE | 25. PRIORITY
32. CLASSIFICATION OF FAILURE
1 ☐ INHERENT 4 ☐ CRITICAL ANALYSIS?
2 ☐ INDUCED 5 ☐ MAJOR 7 ☐ YES
3 ☐ UNKNOWN 6 ☐ MINOR 8 ☐ NO
28. ALERT SUPPLEMENT 0 ☐ NO 1 ☐ YES
D.

33. REPORTABLE ITEM ROUTED TO: NAME | ORGANIZATION OR DEPT. & GROUP

53. CAUSE OF FAILURE, AND/OR CONDITIONS PERTINENT TO THE FAILURE

52. DESCRIPTION OF TROUBLE, ENVIRONMENT, & TEST CONDITIONS

NAME DEPT. & GROUP

NAME DEPT. & GROUP

54. IRIS NARRATIVE (40 CHARACTERS MAXIMUM)

33. PARTS REMOVED

J. 29. LINE NO.	30. PARA NO.	81. RWK CODE	82. PART NUMBER	SERIAL OR LOT NUMBER 83. OLD PART REM/RWK	84. NEW PART INSTALLED	85. REF SYM NO.	86. FAIL. CODE	87. SUPPLIER	88. ENVELOPE OR FRR NO.	K.

36. FINAL DISPOSITION 0 ☐ RETEST OK 2 ☐ REPAIRED 3 ☐ CONDEMNED
37. REPAIRED BY: 1 ☐ DEPOT 2 ☐ MFG. 3 ☐ FIELD
39. REPAIRED BY: NAME DEPT & GROUP

43. REWORK MH RETEST MH TROUBLE SHOOTING MH | 44. REF. DOCUMENT | E. | F.

48. DATE RECEIVED MONTH DAY YEAR | 49. FINAL DISPOSITION OR REPAIR DATE MONTH DAY YEAR | 50. RELIABILITY SIGNATURE | 51. QUALITY SIGNATURE

55. RESULTS, ACTIONS, AND REMARKS.

G.
H.
I.
J.

57. FINAL SUPPLEMENT 0 ☐ NO 1 ☐ YES

56. IRIS NARRATIVE (40 CHARACTERS MAXIMUM)

Figure 2. FRR Form 851-D-1

851-D-1 REV. 2/75

The importance of the failure reporting task is well recognized by the MICRON program management and will be continued by an Autonetics MICRON reliability engineer.

TABLE 6

Failure Reports Initiated

Quarter Ending	Number of Failure Reports Initiated
Phase 2A (N57A-1/2)	
October 1974	5
January 1975	16
April 1975	7
July 1975	4
October 1975	1
January 1976	0
April 1976	0
	33
Phase 2B (EPM-1/-2)	
July 1976	9
October 1976	44
January 1977	64
	117
TOTAL	150

GIDEP ALERTS - The Government-Industry Data Exchange Program maintains a system of advising all participating members of all problems encountered by any member on piece parts, materials, and processes. Information on each problem is disseminated throughout industry on a standard form called an "ALERT".

During the performance of the contract, 460 ALERTS were reviewed to establish whether the problem had potential impact on MICRON. As shown in Table 7, 14 ALERTS were determined to have a potential impact on MICRON. In each case, the ALERT was given to the affected Autonetics engineer for dispensation.

TABLE 7

GIDEP ALERT Status

Quarter Ending	No. of ALERTS Reviewed	No. Applicable to MICRON
October 1974	4	0
January 1975	17	0
April 1975	65	2
July 1975	72	4
October 1975	13	0
January 1976	38	0
April 1976	57	1
July 1976	56	0
October 1976	82	5
January 1977	56	2
TOTALS	460	14

It is deemed very important that this surveillance be continued, particularly during the future MICRON production phase, since a single bad part, if not discovered early in the build cycle, could seriously jeopardize MICRON reliability and cost-of-ownership goals.

2.4 Task 4 - Reliability Tests. This task was deleted per revised statement-of-work dated 20 December 1976.

2.5 Task 5 - Design Reviews. In this task the statement-of-work called for MMC to conduct monthly design reviews at the Autonetics, Anaheim, California facility to discuss the status of the MICRON reliability program. This requirement was clarified by AFAL to mean that MMC should not independently organize formal Design Reviews at Autonetics, but that MMC should actively participate in the Design Reviews scheduled at Autonetics by AFAL, and that MMC should be involved in the informal Design Review process at Autonetics. Accordingly, during the contract, MMC participated with viewgraph presentations in nine Design Reviews, chaired by AFAL, as follows:

July 23-25, 1974
February 18-21, 1975
August 19, 1975
October 6-8, 1975
February 10-12, 1976
August 11, 1976
October 21, 1976
December 15, 1976

Informal Design Reviews were an on-going, almost daily, event with MMC and Autonetics during our location at the Autonetics plant in Anaheim. At least once per week, and sometimes many times daily, MMC would meet with the knowledgeable engineer(s) in the particular design areas being reviewed at that time. At certain periods, the design was changing often requiring nearly constant surveillance to keep abreast of the new design developments.

It was necessary for MMC to maintain continuous surveillance of the design because of the MICRON electronic parts list which we originated and published at frequent intervals. Also, reliability assessments were being continually updated. This required many Design Reviews to determine the design status before such assessments could be made. Figure 3 shows a completed program schedule which was kept updated by MMC during the program. Line 15 shows that design reviews were performed at least once per month.

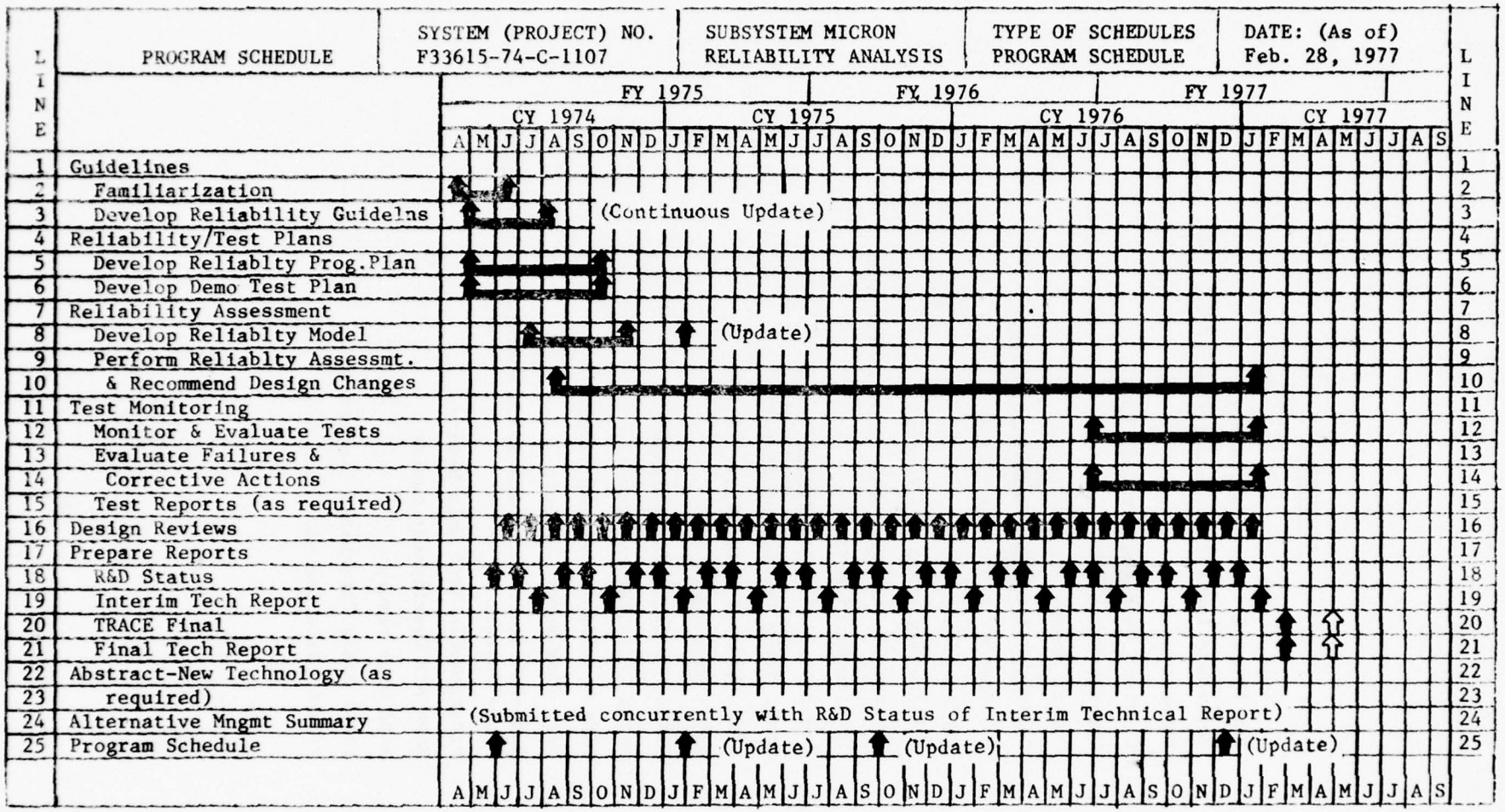

Figure 3. Martin Marietta Corporation - Program Schedule

ACRONYMS

AFAL	Air Force Avionics Laboratory
AIA	Aerospace Industries Association of America, Inc.
AN	Autonetics
CDRL	Contract Data Requirements List
CPC	Ceramic Printed Circuits
DMAC	Direct Memory Access Control
DPU I/O	Dedicated Processor Unit Input/Output
EPM	Engineering Prototype MICRON
ESG	Electrostatic Gyro
FRR	Failure Reporting and Removal
GIDEP	Government-Industry Data Exchange Program
ICs	Integrated Circuits
INS	Inertial Navigation System
LSI	Large Scale Integrated Circuit
MESG	Micro-Electrostatic Gyro
MLB	Multilayer Board
MMC	Martin Marietta Corporation
MOS	Metal Oxide Semiconductor
MSI	Medium Scale Integrated Circuit
MTBF	Mean-Time-Before-Failure
NASA/JSC	National Aeronautics and Space Administration/Johnson Space Center
PROM	Programmable Read Only Memory
RADC	Rome Air Development Center
ROM	Read Only Memory
SSI	Small Scale Integrated Circuit
WPAFB	Wright Patterson Air Force Base

APPENDIX A

RELIABILITY GUIDELINES FOR THE MICRON INS SYSTEM

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TABLE OF CONTENTS (CONTINUED)

SECTION I

INTRODUCTION

Reliability analyses have shown that the reliability of the MICRON IMU is almost wholly dependent on the hybrid microelectronics. Therefore, these guidelines concentrate on the hybrids and on the component parts of the hybrids.

Since the format selected for each section was chosen as that best suited to the subject material, it will be found that the format varies from section to section.

In formulating these guidelines, it was decided to make the guidelines comprehensive; that is, to include practices already being used by Autonetics. The advantage of this approach is that, after the guidelines are worked off with Autonetics, they will then constitute a good baseline reference document of the total reliability practices being implemented on the MICRON program. The document can then be altered and improved based on the experience acquired in Phase 2B, and will eventually define the reliability do's and don'ts for the MICRON production program.

SECTION II

HYBRID MICROCIRCUITS

A. BASELINE HYBRID PROCESS PLAN

Prior to fabrication of the hybrids for the development (Phase 2B) program, a flow chart depicting all the steps of the hybrid processing should be established and the applicable procedures for each step identified by procedure number. Procedures not now in existence should be written prior to the start of hybrid fabrication. After start of fabrication, all changes to the processes should be promptly incorporated into the process plan. A system of traceability is necessary so that the specific hybrid failures which occur during the reliability demonstration testing can be traced to the specific process actually used at the time of manufacture. Otherwise, the cause of the failure, the corrective action, and the reliability estimate cannot be readily established.

B. SUBSTRATES

1) Substrate temperature should be limited to 80°C to minimize temperature dependent failure mechanisms.

2) Substrate thickness should be sufficient to avoid breakage problems.

3) Substrates must not contain contaminants, such as lead, which could effect resistor characteristics.

C. SUBSTRATE LAYOUTS

1) Single level construction is preferred.

2) The substrate layout should avoid thermal concentrations.

3) Pad spacing under passive components must be sufficient to guarantee that shorts cannot be developed by conductive attachment material.

4) Line resistivity shall not exceed .01 ohm per square. Thick film substrates shall have 10 mil edge clearance minimum for conductors, resistors, glass or other elements.

5) Line widths and line spacing on thick film substrates shall be a minimum of 10 mils each.

6) 10 x 10 mil minimum conductor area shall be provided for wire bonds.

7) Wires crossing other wires shall be minimized.

8) The layout design shall provide assurance that no molten overflow from chip mounting can impinge upon wire bonding areas.

D. CONDUCTORS

1) Palladium-gold or platinum-gold is preferred for thick film conductors. Silver is prohibited to avoid migration at conductor-resistor interfaces.

E. THICK FILM RESISTORS

1) Maximum resistor surface temperature shall not exceed 150°C.

2) Screened or deposited resistors are preferred over chip resistors.

3) Resistors shall not be trimmed by use of wire bonds.

4) Use Bismuth-Ruthenium Oxide, Thallium, or Iridium as thick film resistor materials for greatest stability. Palladium and silver should be prohibited because of instability in reducing atmosphere (palladium) and migration (silver).

5) Precise mask preparation is required to provide resistors within acceptable trimming limits.

6) Resistors shall not be trimmed, utilizing Blow Bar technique employing current or voltage pulses.

7) Thick film drying and baking processes should be selected and controlled to avoid outgassing and to provide stability of resistance characteristics.

F. CHIP MOUNTING

1) Chip mounting pads shall extend beyond chip outlines on all four sides, a minimum of 5 mils.

2) Chips shall be eutectically attached whenever possible.

3) Adhesive bonding of chip capacitors and resistors is preferred over solder bonding because of the low capability of solder bonds in a temperature cycling environment.

4) Any active chips and/or any passive chip with an active or metalized mounting surface shall not be mounted over conductors or resistors even though glass insulation is provided.

5) Thick film resistor chip and/or ceramic capacitor with conductive end terminations may be mounted over conductors provided that the conductor run is parallel to the end terminations and that there is adequate clearance to preclude shorting.

G. BEAM LEADS

1) Beam lead push tests are required.

H. BONDING WIRE

1) Wire current carrying capacity shall be adequate for the application. Maximum current in a wire shall not exceed 1×10^5 amperes per square centimeter.

2) Gold wires shall be used.

3) The minimum wire diameter shall be 1.0 mil.

I. WIRE BONDING

1) 100% wire bond pull testing is required.

2) The number of crossover wires, where any single wire both originates and terminates on the substrate, shall be kept to a minimum and in no case to exceed 10% of the total wires.

3) Strapped conductor runs are not allowed.

4) Interconnect wires shall not be capable of coming closer than five wire diameters from another wire, package post, die or portion of the package after a spherical radial distance from the bond perimeter of 5 mils for ball bonds, or 10 mils for ultrasonic and thermocompression bonds.

5) Intra- and interchip, and chip to pinout wire bonding is not permitted.

6) Maximum crossover wire lengths shall be 100 mils, except wires to pinouts may be 150 mils maximum.

7) Gold-aluminum bonding interfaces are undesirable. A monometallic (gold-gold) system is preferred.

J. CONFORMAL COATING

1) A suitable conformal coating is necessary to eliminate the particle contamination problem. The coating shall be selected and tested to prove that flying lead breakage will not occur during temperature cycling.

K. ELECTRICALLY INSULATIVE ADHESIVES

1) The adhesive used for bonding chip capacitors and resistors to the substrates should be chosen with regard to reliability factors such as extent of outgassing, corrosivity, effect of outgassed constituents on uncased semiconductor devices, and retention of bond strength under long-term operating conditions.

2) The use of an adhesive is preferred over solder joining of capacitors. A previous investigation by NASA clearly delineated that solder joined capacitors are susceptible to catastrophic failures during temperature cycling.

3) The adhesive selected for MICRON shall be verified, by tests, as meeting the following guidelines.

Electrical Properties: Stable electrical properties must be maintained over a wide range of temperatures (e.g., insulative adhesives should maintain a volume resistivity greater than 10^{14} ohm-centimeters in the dry condition).

Handling Convenience: Selection should be influenced by factors such as these: storage life and conditions; pot life; whether the adhesive is a single component or two-component system; and whether or not it is available premixed, frozen, and/or in a ready-to-use tube.

Ease of Application: The adhesive must be capable of being applied in controlled amounts and thicknesses and give void-free bonds. Insufficient thickness can result in electrical breakdown, whereas, excessive amounts can produce excessive stresses during temperature cycling.

Flow During Cure: Excessive flow during cure must be prevented to avoid coating of adjacent areas which subsequently must be soldered, or bridging of conductor lines and possibly causing electrolytic corrosion.

Shrinkage During Cure: Excessive shrinkage during cure must be prevented to avoid mechanically stressing components and cracking them or inducing parameter changes.

Component Creep: The tendency of an adhesive component to separate due to capillary action or creep during cure is undesirable due to possible contribution to electrolytic corrosion or degradation of wire bonding.

Outgassing: Both the release of condensable volatiles during cure and continued outgassing after cure are undesirable. Outgassed constituents can adsorb onto electronic components and degrade properties.

Ionic Content: The adhesive must not contain water extractable ionic constituents such as Cl^- or Na^+ which will promote corrosion or electrical leakage between conductors.

Tackiness: The exposed edges of the adhesive must be tack-free to avoid capturing of conductive particle contaminants which can cause electrical failure.

Solvent Resistance: Degradation of bond strength or leaching of adhesive components must not occur due to solvents used in cleaning electronic components, modules, or subsystems.

Corrosivity: The adhesive must not be innately chemically corrosive or electrolytically corrosive to the metallization system used.

Flexibility: The adhesives must be sufficiently compliant to relieve mechanical stresses among thermally mismatched materials to avoid warping or cracking of substrates and components.

Repairability: Because of the requirement for rework, it is desirable that the adhesive bond formed be fracturable at sufficiently low temperature and mechanical force to avoid damaging the metallization or breaking the substrate.

Hydrolytic Stability: The adhesives must not degrade chemically (e.g., revert back to a liquid) on exposure for long periods at high temperature and humidity.

Thermal Stability: The adhesives must not decompose at high temperatures or crack at low temperatures (-65 to +150°C).

Bond Strength: The adhesives must have a sufficiently high initial bond strength and must retain adequate bond strength at maximum use temperature, after exposure to commonly used solvents and high humidity, and after extended aging.

Reliability: Hybrid microcircuits assembled using the adhesive must be able to endure the temperature cycling, thermal shock, and constant acceleration tests defined in MIL-STD-883, and MIL-STD-781.

NOTE: The source of the Section K guidelines is a paper, "Evaluation of Electrically Insulative Adhesives for Use in Hybrid Microcircuit Fabrication", J. L. Licari, K. L. Perkins, and S. V. Caruso; IEEE Transactions on Parts, Hybrids, and Packaging, Vol. PHP-9, No. 4, December 1973. Dr. Licari and Mr. Perkins are with the Autonetics Division of Rockwell International Corporation.

SECTION III

MASTER INTERCONNECT BOARDS

A. DESIGN GUIDELINES

1) The thickness of the through-hole should be not less than 0.0015 inch for good resistance to thermally induced cracking.

2) Heavy-layer copper (2-oz) is preferable to 1/2 and 1 ounce circuits, and the thickness of the layer copper and PTH copper should be approximately matched for good resistance to thermally induced cracking.

3) Thinner boards, in which the volumetric proportion of glass epoxy to copper is minimized, are preferable.

4) The standard land, plated-through connection is superior to both functional land and landless designs from the standpoint of thermally induced cracking.

B. PROCESS CONTROL GUIDELINES

1) The two processes critical to the life of multilayer printed circuit boards are the hole drilling process and the electroplating process, both of which require very close control to insure clean holes and ductile copper.

2) Brighteners should not be used in the electroplating bath since they may cause brittle copper.

3) The electroplating bath should be very closely controlled to avoid both brittle copper and hard copper.

C. TEST GUIDELINES

*1) A test coupon from <u>each</u> production board containing 80 to 100 plated-through holes, connected in series, should be temperature-cycled between -65 and 110°C, and increased electrical resistance should be cause for rejection of the production boards. A few boards should be microsectioned horizontally, to inspect for epoxy smear, and vertically to inspect for cracks.

*2) For a nominally mild temperature environment, 50 temperature cycles are recommended. For more severe applications, 200

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*These are the two "key" guidelines. The other guidelines are directed towards design and process control guidelines necessary to insure the success of these two astericked test guidelines.

temperature cycles are recommended. (The selection of the proper number for MICRON must await definition of the internal MICRON IMU thermal environment.)

3) Acceptance tests should also include temperature shock tests simulating the wave, or the hand soldering operations, since thermally induced warping of the boards tends to cause cracks between the inner copper planes and the plated-through hole.

SECTION IV

INTEGRATED CIRCUITS

A. INTRODUCTION

Parts with established reliability history should be first choice, considering the possibility that parts with the longest history may be superseded by improved techniques of design or processing. Parts without sufficient data must be thoroughly evaluated before they are approved for use.

Established processes and material/process combinations whose failure mechanisms are well-known should be used. New or unique processes, such as amorphous semiconductors, are characterized by a lack of understanding of the basic principles by which they operate. Failure mechanisms, life capability and reliability are unknown.

Parts should be used that are available from several sources in active production. During a long-term program, the probability of a single supplier discontinuing production is increased.

Maximum, practicable use of beam lead technology is emphasized.

B. REVIEW OF SUPPLIER'S DESIGN FEATURES AND PROCESSES

Prior to final selection of the IC suppliers, the candidate ICs should be reviewed for conformance to all, or a majority, of the following design and process guidelines.

Design Guidelines

1) Phosphosilicate glass should be used over the thermal oxide with a maximum thickness of 0.24 micron to getter surface sodium contamination.

2) The supplier should use silicon nitride or other glassification over the chip to protect the SiO_2/Si interface from external sources of channel-including contamination, immobilize residual contamination, and protect the chip surface from handling damage and particulate shorts. Since glass will not adhere satisfactorily to gold, the moly-gold system will require an additional layer of molybdenum atop the gold.

3) The IC should use a monometallic system for chip metalization, interconnect wires, and bonding pads of external leads to eliminate formation of intermetallic compounds that result in poor bonds.

4) The thickness of aluminum metalization must be at least 10,000 Å to avoid oxide step defects, window microcracks, and dangerously thin metalizations.

5) Maximum design-use aluminum current density must be 5×10^4 amp/cm^2 to minimize electromigration effects.

Process Control Guidelines

1) Metalization deposition processes and annealing procedures should be used that result in large uniform grain structures with a minimum grain size of 8 microns to minimize electromigration effects. Wafer should be heated to 300°C or greater during deposition.

2) A planetary deposition system should be used for metalization to eliminate shadowing at oxide steps.

3) The following processes should be reviewed and assurance obtained that they are adequate, stabilized, and under proper control by the manufacturers to minimize contamination and metalization imperfections, and to provide high yield, stability, and precise characteristics.

   a) Thorough wafer cleaning at each process step.

   b) Precise mask layout, dimensional control, alignment, and exposure.

   c) Uniform resistivity of basic wafer.

   d) Purity of photoresist, proper application, spin, and bake.

   e) Thorough resist development and post-development inspection.

   f) Controlled depth, rate, angle, and undercut of oxide etch processes and thorough post-etch inspection.

   g) Thorough resist removal.

   h) Precise diffusion or deposition and drive-in, reoxidation purity.

   i) Precise oxide growth, removal, and epitaxial growth.

4) A production lot should be identified as those parts from a single metalization run, because the metalization deposition process is responsible for numerous failures.

C. INTEGRATED CIRCUIT SCREENING TEST GUIDELINES

The extent of integrated circuit screening by the manufacturer significantly effects costs and, therefore, the screening program is a cost-of-ownership/reliability tradeoff. This tradeoff should determine the desirability (or undesirability) of the following tests.

1) 100% electrical testing and burn-in for a minimum of 168 hours is mandatory for screening out defective devices. For parts requiring higher reliability, consideration should be given to burn-in for longer than 168 hours, or at higher temperatures, because the internal elements of integrated circuits cannot be stressed to their rated capability. Temperatures higher than 125°C should be considered (in anticipation of the new MIL-STD-883).

2) 100% visual inspection to standards superior to that required by the current MIL-STD-883 is required to detect time-dependent failure mechanisms resulting from scratches, pin-holes, residues and improperly controlled processing.

3) Submit a wafer sample from each metalization run to a detailed SEM (scanning electron microscope) inspection to assure uniform and continuous metalization over window cuts and oxide steps, to find any undercutting and water-fall effects from oxide etch, to detect oversintering, and to verify mask alignment. Inspection at the wafer level is the most economical point in the process sequence for performance. Screening tests are not 100% effective in detecting these faults and further costly processing is avoided.

4) Submit a wafer sample from each metalization run to a profilometer test to verify metalization thickness and avoid electromigration problems.

D. APPLICATION GUIDELINES

1) Circuit voltage transients should be limited and static charge precautions should be followed in handling because built-in protective circuits are not generally provided and circuit damage must be avoided.

2) Current-limiting should be provided when interfacing with similar circuits so that power dissipation limits will not be exceeded.

3) Refer to the section on derating for derating criteria.

SECTION V

DISCRETE TRANSISTORS

A. REVIEW OF SUPPLIERS' DESIGN FEATURES AND PROCESSES

Prior to final selection of a transistor supplier, the candidate transistors should be reviewed for conformance to all, or a major part, of the following design and process guidelines.

Design Guidelines

1) The supplier should use planar die constructions. Mesa, grown junction, alloy or germanium types have serious life limiting problems. Mesa constructions, however, are necessary in large power, high voltage, devices.

2) Phosphosilicate glass passivation over thermal oxides and metalization is desirable to getter surface contaminants and protect metalization.

3) Aluminum metalizations should be at least 10,000 Å thick to avoid thinning over oxide steps and be of sufficient cross-sectional area to limit current density to 5×10^4 amps per square centimeter to reduce effect of electromigration (primarily for devices with expanded contacts).

4) Polymer or glass frit die attachments should not be used since they do not afford the thermal conductivity or mechanical strength of eutectic die attachment. (Soft solders for some power devices is unavoidable, but not preferred.)

5) When the die is dielectrically isolated from the case, both die and isolator must be eutectically mounted to afford minimum thermal impedance and maximum strength.

6) Hermetically sealed packages (10^{-8} ATM/cc/sec) must be used for encapsulation of the die since other encapsulants do not afford adequate moisture protection.

7) Dry inert back-fill gas within the package should be present to prevent interaction of the gas ambient with the die materials.

8) Inert non-reactive materials should be used for package and lead materials and platings to preclude package degradation due to corrosion or contamination. They must provide sufficient mechanical strength to withstand handling, shipping and installation environments.

Process Control Guidelines

1) A rigorous pre-cap visual inspection of the die and header assembly is essential to eliminate common assembly defects. Die inspection (preferably at the wafer or die level) should be performed to eliminate defective die.

B. TRANSISTOR SCREENING TESTS

The extent of transistor screening by the supplier affects costs and, therefore, the screening program is a cost-of-ownership/reliability tradeoff. This tradeoff should determine the desirability of the below screening tests and others.

1) Screening tests on 100% of the parts, which include burn-in, HTRB, thermal cycling, mechanical shock, hermeticity, and parametric tests are essential to eliminate defective parts.

2) Qualification tests should be performed once on a group of candidate parts. These tests are arranged in a manner aimed at specific failure mechanisms. The qualification should also include characterization and fingerprinting of the device to establish a baseline for validity of the qualification for future procurements. The fingerprint should be performed on each successive lot to determine conditions which could invalidate qualification. Part type remains qualified as long as screening results, acceptance test results, and part performance are acceptable.

C. APPLICATION GUIDELINES

1) Mechanical installation of the part must provide adequate thermal transfer and preclude severe mechanical stresses.

2) Low leakage devices should be protected from high voltage, low energy transients, such as electrostatic discharges to preclude junction degradation.

3) Refer to section on derating for derating criteria.

SECTION VI

DISCRETE DIODES

A. REVIEW OF SUPPLIERS' DESIGN FEATURES AND PROCESSES

Prior to final selection of diode suppliers, the candidate diodes should be reviewed for conformance to all, or a major part, of the following design and processes.

Design Guidelines

1) Phosphosilicate glass should be used for glassivation of die surfaces. The phosphosilicate is desired because of its characteristic to act as a getting agent for sodium.

2) Laser, chemical or ultrasonic scribing techniques should be used to prevent cracks that occur during diamond scribing.

Process Control Guidelines

1) The part manufacturer should demonstrate process control effectiveness. This should be in the form of records that show increasing or stable yields for the processes in question or in the form of test data that shows decreasing or stable reject rates. Data of this nature should demonstrate that the processes are being controlled effectively. Other results may indicate inadequate process control.

2) The part manufacturer should have in-line check points that verify that the process is in control. An example of this is a lead bond pull test of a sample of units taken from the line periodically. Consistent or increasing bond pull values would be indicative of lead bond process control. Varying or decreasing values would be indicative of either inadequate process control or personnel variations.

B. DIODE SCREENING TESTS

The extent of diode screening by the supplier affects costs and, therefore, the screening program is a cost-of-ownership/reliability tradeoff. This tradeoff should determine the desirability of the below screening tests and others.

1) Testing must be based upon the results of evaluation of the part. Tests may vary from part to part depending upon construction and function. The screen test should include the following in the sequence mentioned.

a) Internal visual;

b) Stabilization bake for 96 hours;

c) Thermal shock;

d) Acceleration (except double slug diode);

e) Hermeticity;

f) High temperature, reverse bias (except silicon controlled rectifiers);

g) Burn-in (may be an a.c. blocking voltage);

h) Radiography; and

i) External visual.

2) Tests designed to detect particles such as weld splatter or solder balls should be implemented. The monitored vibration test and Particle Impact Noise Detection (PIND) test are both effective.

3) High temperature bias must be performed on planar type diodes. The exposure to voltage or current and temperature will detect inversion or accumulation defects.

C. APPLICATION GUIDELINES

1) Stud torque and seating plane flatness should be controlled to prevent excessive stresses in the die/header interface and to promote better heat transfer.

2) Stress relief of leads and interconnecting wires should be provided to prevent damage to the hermetic seal of the part.

3) Refer to section on derating for derating criteria.

SECTION VII

THERMISTORS

It is understood that a specific thermistor has not been selected at this time. It is assumed that a semiconductor resistance sensor, produced by sintering various mixtures, will be used. A MIL-T-23648 thermally sensitive resistor might be an alternative.

A. REVIEW OF SUPPLIERS' DESIGN FEATURES

Prior to the final selection of the thermistors, the candidate thermistors should be reviewed for conformance to all, or a major part, of the following design guidelines.

Design Guidelines

1) The exposed sintered material should be hermetically sealed. Aging of exposed sintered material causes large resistance shifts.

2) Select a supplier with a proven stable device. In the past, thermistors have been relatively unstable devices.

B. THERMISTOR SCREENING TEST GUIDELINES

The extent of thermistor screening by the supplier effects costs and, therefore, the screening program is a cost-of-ownership/reliability tradeoff. This tradeoff should determine the desirability of the following test and others.

1) Burn-in the device for 1000 hours at 150°C if a drift less than one percent is desired. Then measure the temperature resistance curve over the desired operating range. The device is then burned in for 168 hours at 125°C and the temperature vs resistance curve verified. JPL found the foregoing technique to be superior to a temperature cycling test. The preceding 1000-hour burn-in may not be required if the device has a proven stable performance.

C. APPLICATION GUIDELINES

1) Provision should be made to insure careful handling since experience indicates that thermistors are relatively fragile.

2) Refer to section on derating for derating criteria.

SECTION VIII

NI-CD BATTERIES

A. REVIEW OF SUPPLIERS' DESIGN FEATURES AND PROCESSES

Prior to final selection of the battery supplier, the candidate batteries should be reviewed for conformance to all, or a major part, of the following design and process guidelines.

Design Guidelines

1) It should employ a pressure relief valve (200 psi or less) to prevent crew injury in case of battery overpressure. Replace battery if pressure is relieved, because chemical balance is upset and cell case probably distorted. Option: contain battery in a "protective" case.

2) Either the terminal seal braze should be plated with nickel or a nickel-titanium braze material should be used to reduce the probability of electrolyte attacking materials containing copper.

3) The case and cover material should be 304 or 304L stainless steel. These materials have proven satisfactory.

4) The battery should be hermetically sealed to avoid degradation of other parts by the electrolyte.

5) The negative to positive plate area ratio should be at least 1.5:1 so that the negative plate area can absorb the oxygen generated during recharge, preventing battery overpressure.

6) Ceramic-to-metal terminal seals that are more KOH resistant than glass should be used.

Process Control Guidelines

1) Clean areas should be employed during processing and manufacturing to reduce the amount of harmful contaminants. Also, clean lint-free cotton gloves should be used when handling components. Components to be in clean plastic bags when not being processed.

2) The carbonates should be removed and the nitrates content kept down to prevent gas pockets that pop off active material.

3) To remove carbonates, the plates should be flushed after KOH is used in the process to form active hydroxides.

4) Plates should be flushed and brushed prior to installation to remove contaminants.

5) Plates should be coined flat. The supplier should flex and clean plates prior to assembly. An Autonetics resident inspector should examine plates for conformity just prior to cell assembly. These actions will reduce the probability of short due to projection of jagged wire filament through the separator, loose particles of plate material and tab failures.

6) The supplier should weigh each plate to be certain weights are within $\pm$3-1/2% of mean. Also, actual capacitance measurements to check plate matching should be conducted. Mismatched cells can prevent full battery charge.

7) The brazing temperature-time relationship should be controlled to prevent excess dwell during brazing operations that can cause active material penetration of ceramic seals.

8) Vendor process controls should preclude rapid cooling after brazing to prevent cracked ceramics and brazing voids.

9) The cells should be purged of air prior to injecting electrolyte to prevent KOH reacting with CO_2 to form carbonates.

10) The supplier should have established process and test controls for each active element; plates, separators and electrolyte to reduce end product variability.

B. BATTERY SCREENING TESTS

The extent of the battery screening by the supplier effects costs, and therefore, the screening program is a cost-of-ownership/reliability tradeoff. This tradeoff should determine the desirability of the following screening tests.

1) The assembled cells should be subjected to a helium leak check. As an alternative, a check with phenolphtalein is satisfactory.

2) Battery should be subjected, during acceptance test, to a minimum of three charge/discharge cycles, a high impedance short test, and a leakage test. These tests should provide assurance that the basic operating characteristics and construction are satisfactory.

3) X-ray along three axes to find gross battery defects.

4) Conduct a minimum of 30 charge/discharge cycles on assembled cells to minimize infant mortality and to confirm the matching of individual cells. Resident inspection should observe and confirm these tests.

C. APPLICATION GUIDELINES

1) Maintain battery within a -20°C to +22°C temperature range to retard separator deterioration.

2) Limit recharge and overcharge as denoted below to assure longer battery life.

   a) The recharging rates should be limited to the range of C/2 to C/10. (C = rated capacity in ampere-hours.)

   b) The overcharge should be limited to:

      105% C @ 0°C
      115% C @ 25°C
      125% C @ 40°C

3) Plan to replace batteries operating under "semifavorable" usage and environments about every two years.

4) Store Ni-Cd batteries at approximately 0°C in a discharged and shorted condition to obtain a storage life of about five years.

5) Monitor individual cell voltages for indications of cell deterioration and potential replacement requirements.

6) Erase most memory by discharging battery, short for 16 hours, and then recharge if application permits and need arises. Repeated shallow depths of discharge can prevent future fuller depths of discharge ("memory").

7) Design excess capacity into the battery to reduce the percent of depth of discharge and compensate for capacity decrease with age.

SECTION IX

SOLDER JOINTS

Solder joints, which are stressed due to the inadequate provision of lead stress relief, will crack and electrically open during thermal cycling. Therefore, adequate stress relief should be provided for all solder joints and any questionable configurations should be verified by testing for 200 temperature cycles between -55°C and 100°C. It should be noted that slow cycling of solder joint is more severe than a fast, accelerated cycle. This is because, in a slow cycle, the joint undergoes more creep (which is time-related), more recrystallization, and this results in cracking in a fewer number of temperature cycles.

SECTION X

MESG

A. CAVITY

1) The ESG electrode structure of the cavities should be formed from material which is very hard, very dense, has high mechanical strength, low coefficient of thermal expansion, low dielectric loss, and good thermal conductivity.

2) The metalized plating on the inner sphere of the cavity must have very low magnetic susceptibility.

B. BALL

1) To reduce gyro drift, the ESG rotor should be formed from a stable material that can be lapped to provide a repeatably round ball at operating speed and temperature during each operation. That is, during ESG operation the elongation in a line joining the poles (prolateness) is the correct amount to overcome the flattening at the poles (oblateness) caused by spin stress and can be exactly repeated on each spin up.

2) The rotor should have a completely uniform structure of *composition of the material with respect to density* (*i.e.*, no voids, inclusions, or non-uniform compaction of material particles) and low thermal expansion characteristics. Even though a slight axial mass unbalance is desired, the <u>stability</u> of this unbalance coefficient is extremely important, thus, must be controlled.

C. COIL

1) To reduce the delta increase of the ESG internal temperature generated by using the spin coil, the gyro spin coil should be designed for the minimum wattage necessary to perform the spin/despin tasks and the maximum heat transfer <u>away</u> from the cavities and ball.

D. HI-VACUUM PUMP SYSTEM

1) Gaskets in the hi-vacuum system should be electronic grade, annealed copper gaskets, or equivalent; they should be used only once to assure leak-free performance.

2) High vacuum lines should be glass, copper, stainless steel, or nickel tube, which can be sealed off. Joints should be heliarc welded or brazed (flux-free).

3) Opposing flanges of any flange joint in the high vacuum system should be closely inspected for scratches which might provide a leak path.

4) Bolts, nuts and washers that have the same thermo expansion as the flanges should be used for fastening high vacuum flanges.

5) The entire assembled high vacuum system should be checked with a high quality helium leak detector test before using the system.

E. "GETTER"

1) If a "getter" is used to provide the final high vacuum environment for an ESG, care should be taken in selecting the "getter" to prevent introducing residue inert gas molecules that would be detrimental to the gyro operation.

SECTION XI

DERATING GUIDELINES

The following derating factors indicate the maximum recommended stress values and do not preclude further derating. When derating, the designer must: 1) take into account the specification environmental and operating condition rating factors; 2) consider the actual environmental and operating conditions of the application; and then 3) apply the recommended derating factor contained herein. Since the operating characteristics for such parts cannot be guaranteed, it is a good policy to derate generously to provide an additional margin of safety. Where parts are listed, but are not given a specific derating value, a good general practice should also be to derate generously.

A. MICROCIRCUITS

Derating guideline factors for microcircuits are tabulated below:

Type	Derating Factor	Parameter	Applicable Notes
Digital	.80	Output Current	1, 2
	.75	Operating Frequency	
Linear	.70	Bias Voltage	1, 3
	.70	Input Signal Voltage	
	.75	Output Current	
	.75	Operating Frequency	
Voltage	.80	Input Voltage (rated maximum)	1
	.75	Output Current (rated maximum)	
	.60	Power Dissipation (rated maximum)	

NOTES:

1. All microcircuits shall be used at ambient temperatures less than 85°C.
2. This derating factor is not to be used when fan out would be reduced to less than one.
3. Further derate linear IC circuits as follows so that end of life drift characteristics will be considered in product design.
   a) Initial offset voltage, $\pm$1/2 mv
   b) Initial bias current, X2

c) Offset current, X2

d) Open-loop gain, ±20%

e) Slew rate, ±20%

f) Common mode rejection, ±20%

g) Power supply rejection, ±20%

B. TRANSISTORS

Derating guideline factors for tansistors are tabulated below:

Type	Derating Factor	Parameter	Applicable Notes
General Purpose	.50	Power	1, 2
	.75	Current	
	.75	Voltage	
Power	.30	Power	1, 2
	.75	Current	
	.75	Voltage	
Switching	.50	Power	1, 2
	.75	Current	
	.75	Voltage	

NOTES: 1. Junction temperatures for all transistors shall not exceed 110°C for any combination of parameters.

2. Worst-case combination of d.c., a.c., and transient voltages shall be no greater than the derated limit.

C. DIODES

Derating guideline factors for diodes are tabulated below:

Type	Derating Factor	Parameter	Applicable Notes
General Purpose	.50	Power	1
	.50	PIV	
	.50	Surge Current	
	.50	Forward Current	
Rectifier	.30	Power	1
	.50	PIV	
	.50	Surge Current	
	.50	Forward Current	
Switching	.30	Power	1
	.50	PIV	
	.50	Surge Current	
	.50	Forward Current	

Type	Derating Factor	Parameter	Applicable Notes
SCR	.30	Power	1
	.50	PIV	
	.50	Surge Current	
	.50	Forward Current	
Varactor	.50	Power	1
	.75	PIV	
	.75	Forward Current	
Zener	.50	Power	1, 2
	.50	Forward Current	
	(2)	Zener Current	
Reference	.30	Power	1, 2
	.50	Forward Current	
	(2)	Zener Current	

NOTES: 1. Junction temperatures for all diodes shall not exceed 110°C.

2. Zener current should be limited to no more than $I_Z = .5 \left(I_{Z_{max}} + I_{Z_{nom}} \right)$

D. CAPACITORS

Derating guideline factors for capacitors are tabulated below:

Type	Derating Factor	Parameter	Applicable Notes
Fixed			
Ceramic	.50	Voltage	1, 2
Mica Dipped	.60	Voltage	1, 2
Glass	.50	Voltage	1, 2
Porcelain	.50	Voltage	1, 2
Paper	.50	Voltage	1, 2
Plastic	.50	Voltage	1, 2
Tantalum Solid (3 ohms/ volt limiting resistor)	.50	Voltage	1, 2, 3
Adjustable			
Air	.30	Voltage	1, 2
Ceramic	.50	Voltage	1, 2
Glass	.50	Voltage	1, 2

NOTES: 1. The current derating factor is 70% of manufacturer's specified limit.

2. Manufacturer's derating factors shall be applied before using the factors of this document.

3. Ambient temperature shall not exceed 50°C.

E. RESISTORS

Derating guideline factors for resistors are tabulated below:

Type	Derating Factor	Parameter	Applicable Notes
Fixed			
Carbon Composition	.50	Power	1, 2
Insulated Film	.50	Power	1, 2
Wirewound, Precision			
1.0%	.50	Power	1, 2
0.1%	.25	Power	1, 2
Wirewound, Power	.50	Power	1, 2
Thermistor	.50	Power	1, 2, 3
Adjustable			
Wirewound	.70	Rated Current	1, 2, 4
Non-wirewound	.70	Rated Current	1, 2, 4

NOTES: 1. The maximum voltage for all resistors shall be no more than 80% of the MIL ratings.

2. High density packaging may require further derating if ambient temperatures are increased.

3. Thermistors used in other than zero power applications should also have minimum wattage specified for the application.

4. Rated current is defined as:

$$I_R = \sqrt{\frac{P_{max}}{R_{max}}}$$

and by limiting the current to .70 rated current, power is limited to .5 maximum power.

SECTION XII

WORST CASE ANALYSIS

A worst case analysis should be performed concurrently with the design, beginning in the early stages of development. The analysis should consist of a circuit description with schematic, a summary, a functional analysis, a stress analysis, and test results. The summary should include both a tabulation of all functional requirements versus the functional capabilities, and a tabulation of part applied stress levels versus the derated stress limits. No deviations from requirements or deratings should be allowed without justification, review, and approval. The functional analysis is performed to assure the circuit has the capability to satisfy all functional requirements within the required performance and safety margins, under the most unfavorable combination of realizable conditions. Included are input, output, environmental, and packaging conditions, as well as part parameter dispersions including aging and life tolerances. A computer program should be used to the maximum extent for efficiency and reliability of design. The input program and output data should be included in the report. The worst case stress analysis should verify proper application of parts such that the applied stresses do not exceed the derated values of voltages, currents, power dissipation, etc, under worst case conditions. Worst case conditions include power-up and power-down under all phases of circuit operation including manufacturing and system/subsystem test. The results of tests performed to insure satisfaction of performance requirements and existence of required margins should be included in support of the analysis.

ADDENDUM A

CHIP CAPACITOR GUIDELINES - MICRON

1. Chip capacitors should be qualified to ensure basic capabilities.

2. Screening of individual chips, including burn-in in assembled hybrids, thermal shock and high temperature storage, should be performed to the maximum extent possible. This will assure chip capacitors with a minimum probability of defects. It is not realistic to burn-in chip capacitors until installed.

3. The supplier's use of the required processes should be continuous to avoid reliability risks from startup operations.

4. Avoid plastic encapsulated chips which are environment sensitive.

APPENDIX B

RELIABILITY ASSESSMENT FORMATS

Date _____ COMPONENT RELIABILITY CPC _____

Prepared By _____ DATA SHEET - 1 Drawing No. _____

Line Number	Component	Capacitors			Circuit Designator																					
					Transistors										Diodes, Silicon									Resistors		
					NPN			PNP			FET															
		Ceramic	Tantalum	Other	Logic Switch	Linear	Power > 1 W.	Logic Switch	Linear	Power > 1 W.	Logic Switch	Linear	Unijunction	Logic Switch	Small Signal ≤ 500 MA	Power Rect. > 500 MA	Zener Volt Regulator	Thyristor	Varactor; Step Rec; Tunnel	Detector	Mixer	Thin Film	Thick Film	Screen

Figure 1 - Hybrid Reliability Assessment Data Sheet

Date_____ COMPONENT RELIABILITY CPC _____

Prepared By_____ DATA SHEET - 2 Drawing No. _____

Line Number	Circuit Designator: Monolithic: Bipolar, MOS Digital, SSI MSI	Circuit Designator: Monolithic: Bipolar Linear	Circuit Designator: Monolithic: MCS Linear	Circuit Designator: Monolithic: Bipolar Beam Lead	Circuit Designator: Monolithic: Bipolar, MOS Digital LSI	Circuit Designator: Monolithic: Bipolar & MOS Memory	Number of Gates (4 xstrs per gate) or xstrs N_G	Number of Gates (4 xstrs per gate) or xstrs N_T	Number of Lead Terminations Times 2 Except Beam Lead Times 1 N_{LT}	Useful Substrate Area in Inches^2 A_S	Number of Active Contacts on Substrate N_{SC}	Temperature ^oC	Number of Discrete Chips N_{DC}	Other Discrete Parts

Figure 2 - Hybrid Reliability Assessment Data Sheet (cont'd)

Date _____ HYBRID FAILURE RATE PREDICTION Per Mil-Hdbk-217B CPC _____

Prepared by _____ Work Sheet - 1 Drawing No. _____

Column No. 1		2	3	4	5	6	7	8	9
Data Location		Schematics	Page* 2.1.7-1	Schematics	Schematics	Schematics	Table* 2.1.7-2	Work Sheets	Work Sheets
Line Number	Description and Type of Component	Useful Substrate Area in Inches^2 A_S	Processing Failure Rate λ_S	Total Number of Lead Terminations N_{LT}	Total Number of Discrete Chips N_{DC}	Total Number of Film Resistors N_{RT}	Failure Rate of Film Resistors λ_{RT}	Col 6 x Col 7 $N_{RT} \times \lambda_{RT}$	Summation of Col 8 $\Sigma N_{RT} \lambda_{RT}$

Figure 3 - Hybrid Reliability Assessment Work Sheet #1

*Reference Mil-Hdbk-217B

Date _____ HYBRID FAILURE RATE PREDICTION CPC _____

Per Mil-Hdbk-217B

Prepared by _____ Drawing No. _____

Work Sheet - 2

	10	11	12	13	14	15	16	17	18
	Work Sheets	Work Sheets	Work Sheets & Table 2.1.7-1	Work Sheets	Table 2.1.7-3	Work Sheets	Work Sheets	Page 2.1.7-3	Table 2.1.7-4
Line Number	Col 4 + Col 5 + Col 6. $N_{LT} + N_{DC} + N_{RT}$ = N_E	Col 10 ÷ Col 2 = Density Factor N_E/A_S	Use Col 11 for C_2 in Table 2.1.7-1 Substrate Failure Rate λ_C	Col 2 x Col 12 = Density, Elements Per Inch^2 $A_S \times \lambda_C$	Discrete Component Failure Rate (Chip) λ_{DC}	Col 5 x Col 14 = Total Failure Rate Discrete Components $N_{DC} \times \lambda_{DC}$	Summation of Column 15 $\Sigma N_{DC} \times \lambda_{DC}$	Normalized Hybrid Package Base Failure Rate λ_{PF}	Package Style & Materials Hybrid Base Failure Rate Modifier. $\pi_{PF} = 2 + (\frac{N_{SC}-16}{4})(.15)$

Figure 4 - Hybrid Reliability Assessment Work Sheet #2

Date _____ HYBRID FAILURE RATE PREDICTION CPC _____

Per Mil-Hdbk-217B

Prepared by _____ Drawing No. _____

Work Sheet - 3

	19	20	21	22		23	24	25	26	27
	Work Sheets	Table 2.1.7-3	Table 2.1.5-1	Schematics		Table 2.1.5-5/6/7 or 7B	Table 2.1.5-5/6/7 or 7B	Table 2.1.5-4	Table 2.1.7-3	Work Sheets
Line Number	Col 17 x Col 18 = Hybrid Package Failure Rate $\lambda_{PF} \times \pi_{PF}$	Learning Factor π_L	Quality Factor π_Q	Number of Gates (4 transistors = a gate) or Transistors N_G	N_T	Device Complexity Factor (Temp.) C_1	Device Complexity Factor (Environ.) C_2	Temperature Acceleration Factor for 25°C Per Table 2.1.7-3 π_T	Application Environment Factor (1.0) π_E	(Only IC Chips of Col 5) Col 5 x Col 20 x Col 21 x (Col 23 x Col 26) x ** = Microcircuits Failure Rate $\lambda_{P_{microcircuits}}$

Figure 5 - Hybrid Reliability Assessment Work Sheet #3

**Multiply by 2.0 if a [illegible] device in the Bipolar and MOS linear, Bipolar Beam Lead, Bipolar ECL or other MOS device [illegible]ory.

Date _____ HYBRID FAILURE RATE PREDICTION Per Mil-Hdbk-217B CPC _____

Prepared by _____ Drawing No. _____

Work Sheet - 4

	28	29	30	31	32	33
	Work Sheets	Table 2.1.7-5	Table 2.1.7-6	Table 2.1.7-7	Page 2.1.7-1	Work Sheets
Line Number	Summation of Col 3 + Col 9 + Col 13 + Col 16 + Col 19 + Col 27 = Hybrid Base Failure Rate. λ_b	Temperature Acceleration Factor π_{T_2}	Environmental Factor π_E	Quality Factor π_Q	Circuit Function Factor π_F	Col 28 x Col 29 x Col 30 x Col 31 x Col 32 = Hybrid Failure Rate. $\lambda_{P_{Hybrid}} = \lambda_b (\pi_{T_2} \times \pi_E \times \pi_Q \times \pi_F)$

Figure 6 - Hybrid Reliability Assessment Work Sheet #4

MICRON RELIABILITY PREDICTION SUMMARY DATA

Page ___ of ___

DATE: _____

COMPONENT: Integrated Circuits

MODULE (ASSY.) _____

PREPARED BY: _____

FAIL. RATE MODEL (MIL-HDBK-217B) $\lambda_p = \pi_L \pi_Q (C_1 \pi_T + C_2 \pi_E)$

SCHEMATIC/DWG. NO. _____

Line No.	Quantity N	Ckt. Desc. Ident No.	Part Number	MIL Spec. No. (MIL-)	Vendor or MFR Abbrev.	Part Temp. Data °C T_A	T_C	T_J	IC COMPLEXITY DATA: Bipolar	MOS	SSI/MSI*	Linear	LSI *	Memories *	No. Gates	No. Transistors	No. Bits	No. Pins	F/R Model Factors Per "217-B" Table No.: 2.1.5-2 π_L	2.1.5-1 π_Q	2.1.5-5 thru 2.1.5-8 C_1*	2.1.5-4 π_T	2.1.5-5 thru 2.1.5-8 C_2*	2.1.5-3 π_E	Predicted Fail. Rate f/10^6 hrs: Unit F/R λ_P	Total F/R $N\lambda_P$

Total F/R ($f/10^6$ Hrs)

* For SS/MSI, LSI and memories, multiply C_1 and C_2 values by:

1.1 for 26 to 64 pin package
1.2 for > 64 pin package

Figure 7 - Discrete Integrated Circuit Reliability Assessment Work Sheet

MICRON RELIABILITY PREDICTION SUMMARY DATA

Page ___ of ___

DATE: _____

COMPONENT: Transistors

MODULE (ASSY.) _____

PREPARED BY: _____

FAIL. RATE MODEL (MIL-HDBK-217B) $\lambda_P = \lambda_b (\pi_E \pi_A \pi_Q \pi_{S2} \pi_C)$

SCHEMATIC/DWG. NO. _____

Line No.	Quantity N	Ckt. Desc. Ident. No.	Part Number	MIL Spec. No. (MIL-)	Vendor or MFR Abbrev.	Part Temp. Data °C T_A	T_C	T_J	Complexity Data NPN/PNP (N/P)	FET	Linear	Logic Switch	Elect. Stress Voltage Applied (V_{CE})	Rated (V_{CEO})	(Ratio) S_2	Pwr (Watts) Applied	Rated	(Ratio) S	F/R Model Factors Per "217-B" Table No. 2.2.1-6/7 2.2.2-5 λ_b	2.2.1-1 2.2.2.-1 π_E	2.2.1-2 2.2.2-2 π_A	2.2.1-3 2.2.2-4 π_Q	2.2.1-4 π_{S2}	2.2.1-5 2.2.2-3 π_C	Predicted Fail. Rate f/10^6 hrs Unit F/R λ_P	Total F/R $N\lambda_P$

Total F/R (f/10^6 Hrs.)

Figure 8 - Discrete Transistors Reliability Assessment Work Sheet

MICRON RELIABILITY PREDICTION SUMMARY DATA

Page ___ of ___

DATE: _____

COMPONENT: Diodes

MODULE (ASSY.) _____

PREPARED BY: _____

FAIL. RATE MODEL (MIL-HDBK-217B) $\lambda_P = \lambda_b (\pi_E \pi_A \pi_Q \pi_{S2} \pi_C)$

SCHEMATIC/DWG. NO. _____

Line No.	Quantity N	Ckt. Desc. Ident. No.	Part Number	MIL Spec. No. (MIL-)	Vendor or MFR Abbrev.	Part Temp. Data °C T_A	T_C	T_J	Complexity Data: Small Signal (S/S) or Log. SW (L/S)	PWR Rectifier	Zener (Volt Reg)	Avalanche (Volt. Reg.)	Elect. Stress: Voltage Applied (V_R)	Rated (V_R)	(Ratio) S_2	Current or Power Applied (Iop)	Rated (Imax)	(Ratio) S	F/R Model Factors Per "217-B" Table No. λ_b 2.2.4-6 2.2.5-4 2.2.6-3	π_E 2.2.4-1/5-1/6-1	π_A 2.2.4-3 2.2.5-2	π_Q 2.2.4-2/5-3/6-2	π_{S2} 2.2.4-4	π_C 2.2.4-5	Predicted Fail. Rate f/10^6 hrs Unit F/R λ_P	Total F/R $N\lambda_P$

Total F/R ($f/10^6$ Hrs.)

Figure 9 - Discrete Diodes Reliability Assessment Work Sheet

MICRON RELIABILITY PREDICTION SUMMARY DATA

Page ___ of ___

DATE: _____

COMPONENT: Resistors

MODULE (ASSY.) _____

PREPARED BY: _____

FAIL. RATE MODEL (MIL-HDBK-217B) $\lambda_P = \lambda_b (\pi_E \pi_R \pi_Q \pi_V)$

SCHEMATIC/DWG. NO. _____

Line No.	Quantity N	Ckt. Desc. Ident. No.	Part Number	MIL Spec. No. (MIL-)	Vendor or MFR Abbrev.	Part Temp. Data °C T_A	T_C	T_J	Complexity Data: Composition	Film	Wire Wound	Fixed Variable (F) (V)	Thermistor	Elect. Stress: Voltage Applied (Tab. 2.5.5-4)	Rated (Tab. 2.5.5-4)	Ratio S_2	Power Applied	Rated (PR x C.F.)	Ratio-See Tab. 2.5.7-1 thru 2.5.7-3 S	F/R Model Factor Per "217-B" Table No.: λ_b 2.5.1-1/2-1/3-1/4/5-1	π_C 2.5.1-2/2-4/3-2/4/5-2	π_R 2.5.1-3/2-5/3-3/4/5-3	π_Q 2.5.1-4/2-6/3-4/4/5-4	π_V 2.5.5-4	Predicted Fail. Rate f/10^6 hrs: Unit F/R λ_P	Total F/R $N\lambda_P$

Total F/R (f/10^6 Hrs.)

Figure 10 - Discrete Resistors Reliability Assessment Work Sheet

MICRON RELIABILITY PREDICTION SUMMARY DATA

Page ___ of ___

DATE: _____

COMPONENT: Capacitors

MODULE (ASSY.) _____

PREPARED BY: _____

FAIL. RATE MODEL (MIL-HDBK-217B) $\lambda_P = \lambda_b (\pi_E \pi_{CV} \pi_{SR} \pi_Q)$

SCHEMATIC/DWG. NO. _____

Line No.	Quantity N	Ckt. Desc. Ident. No.	Part Number	MIL Spec. No. (MIL-)	Vendor or MFR Abbrev.	Part Temp. Data °C T_A	T_C	T_J	Complexity Data: Ceramic	Tantalum (Solid)	Tantalum (Non Solid)	Glass	-	Elect. Stress (Voltage): Operating	Rated	S Ratio	Glass Cap. Info: Capacitance Value Muf (for π_{CV})	Solid Tant Info: Circuit Resistance OHMS/volt (for π_{SR})	F/R Model Factor Per "217-B" Table No.: λ_b	π_E	π_{CV}	π_{SR}	π_Q	Predicted Fail. Rate f/10^6 hrs: Unit F/R λ_P	Total F/R $N\lambda_P$
																			2.6.3-3 4-3/5.4/ 5.7	2.6.3-1/ 4/5-5	2.6.5-	2.6.5-2	2.6.3-2/ 4-2/5-3/ 5-6		
																					2.6.3-4				

Total F/R ($f/10^6$ Hrs.)

Figure 11 - Discrete Capacitors Reliability Assessment Work Sheet

MICRON RELIABILITY PREDICTION SUMMARY DATA

Page ___ of ___

DATE: _____

COMPONENT: Inductive Devices

MODULE (ASSY.) _____

PREPARED BY: _____

FAIL. RATE MODEL (MIL-HDBK-217B) $\lambda_P = \lambda_b (\pi_E \times \pi_F)$

SCHEMATIC/DWG. NO. _____

Line No.	Quantity N	Ckt. Desc. Ident. No.	Part Number	MIL Spec. No. (MIL-)	Vendor or MFR Abbrev.	Part Temp. Data °C T_A	T_C	T_J	Inductive Device Family: Transformer Pulse	Audio	Power	RF	Coils	Filters	Insulation Class Per MIL-T-27 MIL-C-15305 MIL-T-21038 O Q	A R	B S	V	T	U	F/R Model Factors Per "217-B" Table No. 2.7.1.2 T_{HS}	$T_A+1.1(\Delta T)$ Table 2.7-5 ΔT	Tables 2.7-6 λ_b	2.7-7 π_E	Table 2.7-4 π_f	Table 2.7-3	Predicted Fail. Rate f/10^6 hrs Unit F/R λ_P	Total F/R $N\lambda_P$

Total F/R (f/10^6 Hrs.)

Figure 12 - Discrete Inductive Devices Reliability Assessment Work Sheet

MICRON RELIABILITY PREDICTION SUMMARY DATA

Page ___ of ___

DATE: _____

COMPONENT: Connectors (Mating Pair)

MODULE (ASSY.) _____

PREPARED BY: _____

FAIL. RATE MODEL (MIL-HDBK-217B) $\lambda_P = \lambda_b (\pi_E \times \pi_P) + N\lambda cyc^*$

SCHEMATIC/DWG. NO. _____

Line No.	Quantity N	Ckt. Desc. Ident. No.	Part Number	MIL Spec. No. (MIL-)	Vendor or MFR Abbrev.	Part Temp. Data °C T_A	T_C	T_J	Connector Configuration: Rack & Panel	Printed Wiring Board	Circular	Coaxial, R.F.	Power	Complexity Data: Insert Material A/B/C/D (Tables 2.11-2, 13)	Contact ampere Rating	Contact Pin Size 12/16/20/22 Ga.	Insert temp rise 2.11-4 ΔT	Oper. temp T_{OP}	$T_A + \Delta T$ Cycling rate Cycles/1000 hours f	F/R Model Factors Per "217-B" Table 2.11-5 λ_b	2.11-6 π_E	2.11-7 π_P	No. active pins N	2.11-8* λ_{cyc}^*	Predicted Fail. Rate f/10^6 hrs: Unit F/R λ_P	Total F/R $N\lambda_P$

*Ignore λcyc if "f" (cycling rate) $\leq$ 40 cycles/1000 hours.

Total F/R ($f/10^6$ Hrs.)

Figure 13 - Connectors Reliability Assessment Work Sheet

MICRON RELIABILITY PREDICTION SUMMARY DATA

Page ___ of ___

DATE: _____

COMPONENT: Printed Wiring Boards

MODULE (ASSY.) _____

PREPARED BY: _____

FAIL. RATE MODEL (MIL-HDBK-217B) $\lambda_P = \lambda_b N \pi_E$*

SCHEMATIC/DWG. NO. _____

Line No.	Quantity N	Ckt. Desc. Ident No.	Part Number	MIL Spec. No. (MIL-)	Vendor or MFR Abbrev.	Part Temp. Data °C T_A	T_C	T_J	Complexity Data: Printed Wiring Bd. P_{W_B}	Multi-Layer Board M_{L_B}	No. Plated Thich Holes N	No. Layers N_L	No. Heaters* N_h	F/R Model Factors Per "217-B" (Page 2.12-5): $6(10)^{-6}$ Two-sided Board λ_{b_1}	π_E	$5(10)^{-4}$ Multi-layer Board λ_{b_2}	π_E	Heater* F/R (if applicable) λ_h	Predicted Fail. Rate $f/10^6$ hrs: Unit F/R λ_P	Total F/R $N\lambda_P$

*If heaters are included as an integral part of board assembly; modify F/R model as follows:

$\lambda_P = \lambda_b N \pi_E + \lambda_h N_h$

(where λ_h = _____ $f/10^6$ hrs.)

Total F/R ($f/10^6$ Hrs.)

Figure 14 - Printed Wiring Boards Reliability Assessment Work Sheet

MICRON RELIABILITY PREDICTION SUMMARY DATA

Page ___ of ___

DATE: _____

PREPARED BY: _____

COMPONENT: Miscellaneous

FAIL. RATE MODEL
(MIL-HDBK-217B) _____

MODULE (ASSY.) _____

SCHEMATIC/DWG. NO. _____

Line No.	Quantity N	Ckt. Desc. Ident. No.	Part Number	MIL Spec. No. (MIL-)	Vendor or MFR Abbrev.	Part Temp. Data °C T_A	T_C	T_J	Complexity Data	Elect. Stress		Predicted Fail. Rate $f/10^6$ hrs Unit F/R λ_P	Total F/R $N\lambda_P$

Total F/R
($f/10^6$ Hrs.)

Figure 15 - Miscellaneous Parts Reliability Assessment Work Sheet

APPENDIX C

MICRON RELIABILITY PREDICTION FOR F-16
INERTIAL NAVIGATION UNIT (INU)

TABLE 1

MICRON Reliability Prediction for F-16 Inertial Navigation Unit (INU) - Summary

Item Description	Items Per System	Engineering Prototype Model (EPM) $Fr/10^6$ Hrs.	Production Model $Fr/10^6$ Hrs.
System Electronics Unit (SEU) No. 1	1	61.514	59.259
System Electronics Unit (SEU) No. 2	1	61.744	59.489
System Electronics Unit (SEU) No. 3	1	53.221	50.267
System Electronics Unit (SEU) No. 4	1	145.468	43.656
Dedicated Processor Unit (DPU)	1	3671.057	213.805
External I/O Unit (I/OU)	1	522.250	95.982
Instrument Assembly Unit (IAU)	1	698.087	195.515
Spin Motor Unit (SMU)	1	18.995	14.293
Power Supply Unit (PSU)	1	362.525	43.633
Mechanical Housing Unit (MHU)	1	131.364	64.151
Total Failure Rate		5726.225	840.050
MTBF		175 Hours	1190 Hours

TABLE 1 (CONTINUED)

Subassembly: System Electronics Unit (SEU) No. 1

Item Description	Items Per System	Engineering Prototype Model (EPM) $Fr/10^6$ Hrs.	Production Model $Fr/10^6$ Hrs.
Sample & Hold, Gap Summation	2	15.742	15.548
Differential Amp. & Notch Filter	1	6.994	6.845
MUM Demodulator	1	4.857	4.760
MUM Demodulator Filter	1	0.494	0.400
Servo Network	1	5.034	4.968
MUM Demodulator, Sample & Hold	1	7.444	7.357
Multiplexer	1	2.861	2.670
Modulator	2	11.601	11.304
MLB Discretes	1	6.487	5.407
Total Failure Rate		61.514	59.259
MTBF		16,256 Hours	16,875 Hours

TABLE 1 (CONTINUED)

Subassembly: System Electronics Unit (SEU) No. 2

Item Description	Items Per System	Engineering Prototype Model (EPM) $Fr/10^6$ Hrs.	Production Model $Fr/10^6$ Hrs.
Sample & Hold, Gap Summation	2	15.742	15.548
Differential Amp. & Notch Filter	1	6.994	6.845
MUM Demodulator	1	4.857	4.760
MUM Demodulator Filter	1	0.494	0.400
Servo Network	1	5.034	4.968
MUM Demodulator, Sample & Hold	1	7.444	7.357
Multiplexer	1	2.861	2.670
Modulator	2	11.601	11.304
MLB Discretes	1	6.717	5.637
Total Failure Rate		61.744	59.489
MTBF		16,196 Hours	16,810 Hours

TABLE 1 (CONTINUED)

Subassembly: System Electronics Unit (SEU) No. 3

Item Description	Items Per System	Engineering Prototype Model (EPM) $Fr/10^6$ Hrs.	Production Model $Fr/10^6$ Hrs.
A/D Converter	1	6.767	6.625
50 KHz Buffer & EMA Power Supply	1	8.250	8.139
Sequencer No. 1	1	5.005	4.825
Sequencer No. 2	1	3.171	3.109
Suspension Timing Generator	1	2.751	2.664
EMA Signal Filter & Data Terminal	1	4.530	4.377
Precision Xtal Osc. & Gap Monitor	1	4.082	4.009
D.C. Reference & Preload Modulator	1	8.454	8.361
Ladder Network	1	1.685	1.633
MLB Discretes	1	8.526	6.525
Total Failure Rate		53.221	50.267
MTBF		18,790 Hours	19,894 Hours

TABLE 1 (CONTINUED)

Subassembly: System Electronics Unit (SEU) No. 4

Item Description	Items Per System	Engineering Prototype Model (EPM) Fr/10^6 Hrs.	Production Model Fr/10^6 Hrs.
Spin Motor Controller	1	4.542	4.431
Temperature Controller	1	5.487	5.334
Calibration Constant Storage No. 1	1	15.061	14.923
Calibration Constant Storage No. 2	1	2.121	1.997
MLB Discretes	1	118.257	16.971
Total Failure Rate		145.468	43.656
MTBF		6874 Hours	22,906 Hours

TABLE 1 (CONTINUED)

Subassembly: Dedicated Processor Unit (DPU)

Item Description	Items Per System	Engineering Prototype Model (EPM) Fr/10^6 Hrs.	Production Model Fr/10^6 Hrs.
Central Processor	1	1316.140	88.578
Processor Input/Output	1	1964.205	99.281
Processor Input/Output	1	390.712	25.946
Total Failure Rate		3671.057	213.805
MTBF		272 Hours	4677 Hours

TABLE 1 (CONTINUED)

Subassembly: External Input/Output Unit (I/OU)

Item Description	Items Per System	Engineering Prototype Model (EPM) $Fr/10^6$ Hrs.	Production Model $Fr/10^6$ Hrs.
Converter Module -	1	95.719	60.536
Synchro Reference Generator	1	3.784	5.437
Synchro Bite	1	1.349	1.983
DAC Amplifier	1	6.734	6.634
Synchro DAC	3	9.923	11.859
Synchro Buffer Amplifier	3/6	12.621	20.803
MLB Discretes	1	61.308	13.820
Data Terminal	1	426.531	35.446
Transmitter/Receiver (Redundant)	2	73.510	4.473
Decoder (Redundant)	2		
Encoder	1	30.879	1.880
MLB Discretes	1	322.142	29.093
Total Failure Rate		522.250	95.982
MTBF		1915 Hours	10,419 Hours

TABLE 1 (CONTINUED)

Subassembly: Instrument Assembly Unit (IAU)

Item Description	Items Per System	Engineering Prototype Model (EPM) Fr/10^6 Hrs.	Production Model Fr/10^6 Hrs.
MESG/Spin Motor	2	169.864	19.314
EMA Assy/Digitizer	3	279.303	54.081
Charge Amplifier	16	99.248	98.032
IAU Assy/Twist Capsule	1	19.908	18.480
Charge Amplifier Assy.	2	129.764	5.608
Total Failure Rate		698.087	195.515
MTBF		1432 Hours	5115 Hours

TABLE 1 (CONTINUED)

Subassembly: Power Supply Unit (PSU)

Item Description	Items Per System	Engineering Prototype Model (EPM) Fr/10^6 Hrs.	Production Model Fr/10^6 Hrs.
Current Limiter & Pre-reg., Assy No. 1	1	78.064	8.860
Regulator, Assy No. 2	1	99.771	11.865
DC-DC Converter, Batt. Charger Mon, & 28 V. Switch, Assy No. 3	1	112.679	14.060
High Voltage Switch	1	72.011	8.848
Total Failure Rate		362.525	43.633
MTBF		2758 Hours	22,918 Hours

TABLE 1 (CONTINUED)

Subassembly: Spin Motor Unit (SMU)

Item Description	Items Per System	Engineering Prototype Model (EPM) $Fr/10^6$ Hrs.	Production Model $Fr/10^6$ Hrs.
Spin Motor Power Pre-Amp & Logic	1	5.174	5.012
Spin Motor Amp Assy -1	1	1.762	0.468
Spin Motor Amp Assy -11	1	1.768	0.512
Spin Motor MLB Assy	1	10.291	8.301
Total Failure Rate		18.995	14.293
MTBF		52,645 Hours	69,964 Hours

TABLE 1 (CONTINUED)

Subassembly: Mechanical Housing Unit (MHU)

Item Description	Items Per System	Engineering Prototype Model (EPM) Fr/10^6 Hrs.	Production Model Fr/10^6 Hrs.
Drive Motor Relay Module	1	41.239	9.394
Mechanical Housing Module	1	90.125	54.757
Total Failure Rate		131.364	64.151
MTBF		7612 Hours	15,588 Hours

APPENDIX D

MICRON ELECTRONIC PARTS LIST

AD-A042 987 MARTIN MARIETTA AEROSPACE DENVER COLO DENVER DIV F/G 17/7
MICRON RELIABILITY ANALYSES.(U)
JUN 77 R W BURROWS, R A HOLTZ F33615-74-C-1107
UNCLASSIFIED MCR-74-164 AFAL-TR-77-62 NL

2 OF 2
AD A042987

END
DATE FILMED
9-77
DDC

DATE July 15, 1976

PART NAME CAPACITORS (Ceramic)

PHASE 2B EPM CONFIGURATION

BY Ray A. Holtz

N73 REVISION 2, 7-20-76

	DPU						I/OU									IAU						SMU				PSU					MPU			
							CONVERTER MODULE							DATA TERMINAL																					
COLUMN NUMBER	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68
UNITS PER SYSTEM	1	1	1	1			1	1	1	1	2	3		1	2	2	1		2	3	16	1	2		1	3	1		1	2	1	1		1	1		
NUMBER OF PARTS / PART TYPE	MLB DISCRETES	CENTRAL PROCESSOR	PROCESSOR MEMORY	PROCESSOR INPUT/OUTPUT		DPU TOTAL	MLB DISCRETES	DAC AMPLIFIER	SYNCRO REFERENCE GENERATOR	SYNCRO BITS	SYNCRO DAC	SYNCRO BUFF. AMP.	CM TOTAL	MLB DISCRETES	TRANSMITTER/RECEIVER	DECODER	ENCODER	DT TOTAL	MC80/SPIN MOTOR	EMA ASST/DIGITIZER	CHAROS AMPLIFIER	IAU ASSEMBLY/ TEST CAPSULE	CHAROS AMP. ASSY.	IAU TOTAL	SPIN MOTOR PWR PRE-AMPLIFIER & LOGIC / SPIN MOTOR AMPLIFIER ASSY.	SPIN MOTOR MLB ASSY.		SMU TOTAL	CURRENT LIMITER & PRE-REGULATOR	REGULATOR	DC/DC CONVTR & BATT CHGR, MCM, 28VDC SW.	HIGH VOLTAGE SWITCH	PSU TOTAL	DRIVE MOTOR RELAY MODULE	MECH. HOUSING UNIT	MPU TOTAL	TOTAL ALL SUB-TOTAL COLUMNS THIS PAGE
250R11W153MP															1			2																			2
250R11W103PP																	1	1																			1
250R15W333PP															4			8																			8
500R11N331JP															1			2																			2
500R11N680JP												4	12																								12
500R11N5R6KP																									3			3									3
500R11N101KP								10		3	8		29								1			16													45
500R11N470KP																					1			16													16
500R11N220MP																					1			16													16
500R11W511JP																									3			3									3
500R11W103KP										6			6																								6
500R11W331KP									1				1																								1
500R11W332KP												4	12																								12
500R11W472KP									1				1																								1
500R11W103PP							4	3	2	3			15								1			16	3			3									34
500R15W203FP							4						4																								4
500R25N402JP																					1			16													16
500R25W104JP												4	12																								12
701A105X							2						2																								2
3943X7R504K300FS																													2			2					2
592C47R124K300FS																															4	4					4

Figure 1. MICRON Electronic Parts List

APPENDIX E

BEAM LEAD TECHNOLOGY REVIEW

June 1975

BEAM LEAD TECHNOLOGY REVIEW

James Beall
June 1975

Scope

This review summarizes the current status and the projected future for beam lead semiconductor devices, identifies problems and tradeoff considerations for feasibility assessment, and presents guidelines. This review is based primarily on telecon surveys of both beam lead device suppliers and hybrid manufacturers/users.

Background

The development of the beam lead sealed-junction process (Lepselter Process) at Bell Laboratories created a new technology capable of solving many problems with hybrid circuits. The gold metallization and beam interconnects provided a mono-metallic interconnect system in a hybrid circuit eliminating problems such as purple plague and Kirkendahl voiding. The higher activation energy of gold (Au = 1.79 ev, Al - 1.1 ev) reduces metal migration problems due to high film current density. With the beam lead chip being hermetically sealed, it can be tested and screened to the same level as hermetically packaged standard chips, providing an improvement in hybrid circuit performance and reliability and a reduction of weight and size.

The acceptance and utilization of beam lead devices was initially fairly vigorous, but this has waned due to problems of limited availability of part types (selection and quantity) and the lack of multiple sources of supply. In addition, it was not feasible to completely test and screen devices (a.c. parameters, temperature and powered or biased screen tests); there is dimensional non-compatibility between suppliers of the same part type; it is difficult to provide conductive particulate contaminant protection; and device handling and circuit assembly processes have not yet been fully developed. These problems are discussed herein.

One area which currently lacks definition is the relative reliability of beam lead devices to standard chip devices. A reliability

study of beam lead devices, RADC Report RADC-TR-75-50, "Reliability Study of Beam Lead Sealed Junction Devices" was recently conducted by Hughes Aircraft Company. This report contains some valuable data, but has triggered a wave of controversy within the industry. A conclusion that beam lead devices are less reliable than standard chip devices has been strongly disputed by most users of beam lead devices. A great quantity of reliability data has been developed by Bell Laboratories. However, this data, from the testing of Bell Laboratories and Western Electric devices, is not necessarily equatable to the devices available from the other suppliers. There has been a limited amount of other reliability data developed by beam lead device users. These data are generally directed towards specific applications and is limited in scope, but the results indicate reliability ranging from equal to superior as compared to standard devices.

This review was undertaken to provide a current picture of beam lead technology. It is not expected to answer all technical, application, or reliability questions, but it does furnish a basis for additional follow-up work.

Suppliers Surveyed

The following suppliers were contacted:

Motorola Semiconductor	- Mesa, Arizona
Raytheon Semiconductor	- Mountain View, California
RCA Solid State Division	- Somerville, N. J.
Texas Instrument Semiconductor	- Dallas, Texas

Both beam lead production and marketing personnel were contacted to gather information for this survey.

Supplier Survey Summary

1. What specific part types are currently available in beam lead:

Motorola - Promised, but not received as of this date.

Raytheon - A beam lead product catalog was supplied which was dated April 1974. This catalog identified the following:

Quantity of Part Types/Family	Part Family
7	Diodes
5	N Channel FET's
40	Bipolar Transistors
7	Zener Diodes
12	Linear Circuits
14	DTL Digital Circuits
38	TTL Digital Circuits
39	Low Power Schottky Clamped TTL Circuits

2. What are typical delivery times?

Motorola: 12-16 weeks from receipt of order to completed standard devices. Could be 8 weeks if device is currently running on the production line. These times represent production time required for standard products and additional time must be included for additional inspection and testing requirements. Current production volume is low due to low beam lead interest.

Raytheon: 12-16 weeks to produce standard products in quantities of 2000-5000 pieces. Larger quantities (10,000-70,000 pieces) require increased times. Presently shipping 90,000 to 100,000 beam lead devices per month. Additional time must be included for Hi-Rel inspection and testing requirements.

RCA: 6-10 weeks to produce completed standard devices, depending on device type. Additional time must be included for added inspection and testing

requirements. They are presently producing large quantities of beam lead devices, but estimates were not available.

TI: 4-8 weeks for normal delivery. Varies from this time depending on customer requirements. For example, beam lead devices currently being supplied for the Trident Program have an approximate delivery time of 42 weeks. Quantities up to 100,000 can currently be handled with no processing problems with exception of 100% visual inspection. Visual inspection capability will be doubled in September 1975. The present estimated beam lead production is 200,000 devices per month.

Discussion

The delivery times requested were for standard beam lead devices which have received the standard supplier inspection and testing. This was done to eliminate confusion due to large variations in additional inspection and screening requirements from customer to customer. The delivery times quoted are typical times to provide an estimate and these times would likely increase for more complex circuits. More accurate delivery times can be obtained from the supplier for specific device types and inspection/screening requirements. It is recommended that the beam lead delivery schedules include substantial margin for developing unique specification requirements. For example, beam attachment verification criteria, and packaging for shipment, must be determined and specified.

An estimated lead time, from time of order to receipt of devices for production, would be 52 weeks. This estimate is for a high reliability part and includes manufacturing, inspection, 100% wafer level d.c. electrical testing and sample qualification testing. This lead time would likely increase further if d.c. electrical testing is required upon receipt. If so, this requires devices be delivered in wafer form with die

held in place on a sapphire slide by low temperature wax. The die is positioned face down in this wax, therefore, requiring front side (active side) 100% visual inspection be performed by the customer. This problem will be resolved once a beam lead device carrier is available.

3. What screening levels have you delivered to:

Discussion

The suppliers will supply to MIL-STD-883 level A or B requirements. The majority of customers have identified screening levels and criteria which has been developed around their specific application requirements. Therefore, no standard screening criteria has been developed beyond the MIL-STD-883 criteria. This may require the identification of additional screening criteria depending upon specific application requirements. Additional criteria to be considered for screening is discussed in the User Survey Summary.

4. What visual inspection and electrical testing is normally provided?

Motorola: The standard visual is MIL-STD-883 level B on 100% basis for front and back side. Motorola's internal criteria is similar to 883, Method 2010.2. Motorola will provide us a copy of their backside visual criteria if not considered proprietary. This information has not been received as of this date.

Electrical testing consists of 100% d.c. wafer probe at room temperature. A.C. and temperature testing is performed only on a sample basis with devices installed in an open package. They are currently working under contract with Lockheed to develop a carrier for beam lead IC devices. It will probably be similar to a Barnes type carrier which will be compatible with standard test equipment. The maximum temperature capability should be in the range of 250°C. Development is due to be completed by the end of 1975.

A sodium ion test has been performed for some customers. This test checks the integrity of the nitride passivation by exposing the

device to sodium ions and then placing the device in an HTRB test at 300°C for 48 hours.

Raytheon: Normal visual inspection is performed to MIL-STD-883, Level B. They will perform to Levels A or C where needed.

Normal electrical testing is 100% d.c. at 25°C with guard bands to assure parameters meet the limits at temperature extremes. They can perform temperature testing on some wafers and on some devices in carriers. They prefer not to perform temperature testing and it is not a routine procedure. They cannot provide a.c. testing at wafer level test. If a.c. performance must be demonstrated, devices are installed in a standard package and tested on a sample basis.

They have developed a carrier for four beam devices and these are being used extensively for devices being supplied to NAR Autonetics. Work is currently in progress to develop a carrier for 14 beam devices and it should be available for use in late 1975. This development is primarily for devices Raytheon is supplying to the Trident Program.

Burn-in and life testing is accomplished on a lot sample basis. The sample is bonded to an appropriate package and tested like a standard packaged part. As carriers for beam lead devices become available, burn-in and life testing can be accomplished without the use of a standard package.

A nitride quality test is performed using an etch rate technique. This is a routine test which is used as an in-line process control.

A sodium contamination test is used to verify the integrity of the nitride passivation. Devices are mounted in packages, exposed to sodium ions, and placed in an HTRB test. This is a quality control test which is routinely performed each month.

RCA: Visual inspection criteria was not obtained. Normal electrical testing consists of 100% d.c. at room temperature. Also, when possible, a.c. tests are simulated by using delta d.c. testing. No temperature testing is performed on the wafer. This is due to the use of low-temperature wax which is used to hold the separated die in wafer order on a sapphire disc.

They are working on a beam lead carrier development contract from Lockheed for the Trident Program. Development completion appears to be 6 to 8 months away. The goal is a 250 to 300°C temperature capability.

They use the etch rate technique to check the silicon nitride passivation quality, and the sodium ion penetration test is used to check the silicon nitride integrity.

TI: Visual inspection standard at TI consists of 100% backside visual on all devices. Front side visual consists of three categories: 1) no front side visual, 2) sample front side to an LTPD = 15, and 3) 100% front side. The main purpose of the backside visual is to make sure the nitride passivation lip extends past silicon edge. This lip-to-silicon interface provides the hermetic seal for the die surface. TI's inspection criteria for both front and backsides was obtained and is presented as Appendix 3.

Normal electrical testing consists of 100% d.c. test of wafer at room temperature with guard bands for temperature and probe resistance. They have no capability to test wafer or chip over extended temperature range and no capability to perform a.c. testing on wafer or chip. Testing for temperature and a.c. verification is done on sample packaged chips as required.

TI has not utilized any beam lead carriers. They are currently developing a carrier for 14 lead B/L devices and feel it will be available for utilization by 1976. They anticipate the carrier will be capable of withstanding operation at about 250°C.

TI performs beam hardness testing when required by a customer, but they feel that this has little value and does not provide assurance of good bondability. Hence, they do not perform it as an in-house process control test. They perform the nitride etch rate test only when required by a customer and do not use it as a process control test.

Discussion

The availability of beam lead carriers will provide an obvious advantage by allowing a.c. parametric testing, testing over the operating

temperature range and device screen testing. This has long been a problem with standard chips and can become a significant cost factor for complex hybrid circuits where these tests must be run at the hybrid level to accomplish this screening. Circuits failing this screening must be reworked and retested or discarded. Also, testing at this stage is more complex and time consuming.

The temperature range of the carrier will be the determining factor for the amount of additional testing that can be performed. For example, a carrier limited to room ambient operation would allow a.c. parametric testing; a carrier capable of -55°C to +125°C would allow d.c. and a.c. parametric testing over the full military temperature range, and a carrier capable of operating at 200°C and above would allow high temperature burn-in, HTRB and life test screening. However, even the most temperature limited carrier would allow some improvement in beam lead device testing.

5. What metal system do you use and what are the typical thicknesses?

Motorola: The Bell Laboratories metallization system is used. The typical thicknesses are:

Platinum (Silicide in windows)	- Not obtained
Titanium	- 1500 Å
Platinum	- 1500 Å
Gold Interconnect	- 2 microns
Gold Beams	- 12-15 microns

Raytheon: The Bell Laboratories metallization system is used. The typical thicknesses are:

Platinum (Silicide in windows)	- Not available
Titanium	- 1000-1500 Å
Platinum	- 1000-1500 Å
Gold (deposited)	- Up to 1000 Å
Gold (plated)	- Over 1000 Å and up to 13,000 Å dependent on device current requirements
Gold Beams	- Plated, and are 13 to 25 microns

RCA: The Bell Laboratories metallization system is used. The typical thicknesses are:

Platinum (Silicide in windows)	- Not obtained
Titanium	- 1200 to 1500 Å
Platinum	- 1200 to 1500 Å
Gold Interconnect	- 2 to 3 microns
Gold Beams	- 12.5 microns

TI: The Bell Laboratories metallization system is used. They are no longer making the TI metal system of Titanium-Tungsten-Gold. They were manufacturing both systems up to a year ago when both facilities were combined into one, and only the Bell system is now produced. The typical thicknesses are:

Platinum (Silicide in windows)	- Not obtained
Titanium	- 1400 Å
Platinum	- 1500 Å
Gold Interconnect	- 1 to 6 microns
Gold Beams	- 10 to 18 microns

Discussion

One of the concerns stated in the RADC/Hughes report were the differences found in the metallization thicknesses between suppliers of similar devices. The typical thicknesses provided for this review show some differences. However, these values were typical estimates for all part families and not one part type. To obtain a more realistic comparison, actual thickness measurements should be made on an individual part type from different suppliers. The significance of differences between suppliers is not known. They could affect interconnect or beam adhesion strength, thermal impedance, beam bonding schedules and even be of no significance. The point is that the presence of differences is not important, unless they have an affect on assembly, performance and reliability.

6. What passivation system do you use and what are the typical thicknesses?

Motorola: Silicon dioxide is used for the standard masking and diffusion process. The typical thickness is from 5000 Å to 7500 Å. Silicon nitride is used to provide a hermetic seal for the die surface. Its typical thickness is 2000 Å. Also, to provide scratch protection for the interconnect metallization and eliminate interconductor shorts due to conductive particles, Motorola is proposing, on the ECOM Program, the use of low temperature glass passivation over the die surface and interconnect metallization. The ECOM Program is a part development and standardization contract awarded to Motorola by the Army (ECOM-Fort Monmouth). This glass passivation will not adhere to the gold metal and will likely crack due to differences in coefficients of thermal expansion. Also, it will not provide a moisture barrier, which is a subject that will be discussed later in this report.

Raytheon: Silicon dioxide is used for providing masking for the diffusion process and die surface passivation. The typical thicknesses range from 1000 Å to 4000 Å depending on the specific location on the die. Silicon nitride is used to provide the hermetic seal for the die surface. The typical thickness is 1500 Å.

RCA: Silicon dioxide is used for diffusion masking and die surface passivation. The typical thicknesses are 6000-8000 Å and represents 4 to 6 cumulative sequential oxidation steps. Silicon nitride is used to provide the hermetic seal for the die surface. The typical thickness is 1800 Å to 2000 Å.

TI: Silicon dioxide is used for the die surface passivation. The typical thicknesses were not obtained. Silicon nitride provides the hermetic seal for the die surface and the typical thickness is 2000 Å.

Discussion

The silicon nitride process is one of the key attributes of the beam lead process. It provides the barrier to isolate the surface from

contaminants which would adversely affect the reliability of the device. It is an effective barrier to sodium and heavy metal ions which, if allowed to reach the surface, would catastrophically influence the device performance. Therefore, the integrity of the silicon nitride is key to the reliability of the device. It must be free from cracks, pin holes, flaws, and etching defects which would weaken and violate its integrity.

7. What new beam lead part types do you anticipate being available in the next 6-12 months?

Motorola: They have won a study/development program from the Army (ECOM at Fort Monmouth). This program will develop 35 beam lead devices. Besides this development, a program objective is to initiate industry standardization and to stimulate interest in the use of beam lead devices. The program duration is two years. During the first six months, five prototypes will be developed for each part type. During the following 18 months, yield improvements will be developed and demonstrated by device deliveries and standardization of beam outs and chip size will be initiated between Motorola and other suppliers. The yield improvement goals are 20% for discretes, 10% for MSI and 5% for arrays. The following part types are to be developed:

<u>Diodes</u>	
1N746	1N5314
1N748	
<u>Transistors</u>	
2N2484	2N3639
2N2907A	2N3725
2N3251	2N3960
2N3467	2N4260
2N3501	2N5115
2N3635	
<u>TTL</u>	
5400	5410
5401	5440
5404	5473
5405	

A12

Low Power Schottky Clamped TTL

54LS04	54LS138
54LS08	54LS193
54LS21	54SL194
54LS32	54LS196
54LS73	54SL197
54LS74	54LS253
54LS86	

60 Gate Array

A810A

Raytheon: They are presently expanding their 54LS line of parts. New development is mostly customer oriented with some company funding. Raytheon maintains that they can produce anything in beam lead that they are presently producing in standard chips. The development cost ranges from $10,000 to $50,000 per type, depending on the complexity of the device.

The following parts have been presently released to production:

54LS00*	54LS10**	54LS12**
54LS01*	54LS11**	54LS15**
54LS03*		

* In high volume production
** Presently producing samples

To production in July 1975:

54LS04	54LS153
54LS05	54LS253

To production in September 1975:

54LS194	54LS195	54LS295

Estimated for October 1975:

54LS02	54LS27	54LS74

Future plans for 1976 (dependent on customer requirements):

54LS138	54LS156	54LS197
54LS139	54LS185	54LS255
54LS155	54LS196	

RCA: New beam lead device development is primarily customer contract work where the customer pays for the development. An estimate of

developmental cost would not be provided as it was felt to be too dependent on many conditions.

TI: They presently do not have any firm plans to develop new beam lead devices in either discrete or in integrated circuits. The problem is they do not know what customers want in the future. There are no plans to develop beam lead C/MOS devices. It typically costs about $20,000 to develop a beam lead integrated circuit from an existing chip.

Discussion:

One of the limiting factors in the application of beam leads is the limited number of available part types. The number is continuing to grow, but its growth is funded primarily by the device users. Therefore, the parts being developed are oriented toward the specific application requirements. To date, this has been, for the most part, the development of radiation-hardened device types, particularly in the integrated circuit area. This does not restrict the use of these devices, but it does involve more complex processing and tighter controls, and this results in more costly devices.

8. Is beam lead production continuous or as required?

Motorola: Because the current demand is low, the impression was presented that beam lead production is not presently continuous, but on an as-required basis.

Raytheon: The production line for beam lead is running continuously 5 days/week. They are currently shipping 50,000 to 100,000 chips per month. A second shift operation is utilized on an as-needed basis. The beam lead line is profitable (operating in the black).

RCA: Their beam lead line is in full-time operation. Would not comment on the production quantities except that beam lead devices for another RCA division runs about 250,000 per year.

TI: They have been in continuous beam lead production since 1968 when they started supplying to the Safeguard Program. The beam lead

line is in continuous operation. Estimated beam lead devices shipped is about 200,000 devices per month. Specific device types may be "on-off", as required by customers.

Discussion:

The beam lead production level is a significant consideration in that the greater the production rate, generally the better the quality; i.e., improved yields, tighter parameter distributions and more consistent process control. The production level is determined by the market demand which has been growing at a slower rate than was predicted several years ago.

9. How does the beam lead future look from your point of view:

Motorola: The future for beam leads at Motorola is good because of the ECOM study program. The present demand for beam lead is low, but the volume should pick up in the next 12-18 months. There are no plans for C/MOS beam lead in the future. Plans for future development by Motorola (excluding ECOM parts) have not been defined.

Raytheon: Their opinion is that beam leads will never replace standard chip and wire technology. It will probably be utilized primarily to support programs where high reliability is required. In addition to the reliability consideration for complex hybrid circuits, beam leads are less expensive than chip-and-wire for multiple lead bonding and for rework. Multiple lead bonding for beam lead devices is a reality, but it is important to control the thickness of the metallization to which you are bonding the beam lead device. This is a particularly important factor for thick-film substrate circuitry.

RCA: The future market appears stable with a gradual increase, probably a linear, rather than an exponential, rate of increase of about 2 to 3% per year. The beam lead device has not caught on as it was predicted to have. It is felt that it will remain a small percentage of the semiconductor market. Beam lead is not a main stream technology such that more advanced types of devices will be supplied as beam lead;

e.g., high performance OP amps, comparators, and D/A convertors. RCA is using the same die passivation and metallization system without beams for their plastic PAK devices. This is their "gold chip" line and uses T/C gold wire bonds. Test data has shown good reliability to date and some data has been obtained from Panama Canal Zone testing.

TI: They feel that as hybrid circuits become more complex, the use of beam lead devices are more desirable than chip-and-wire because they are easier to rework, have better reliability and are less expensive to install. If a hybrid circuit contains 10-15 chips the cost of beam lead versus chip-and-wire is about equal. For circuits with more than 15 chips, the use of beam lead becomes less expensive than chip-and-wire. The demand for beam lead devices is increasing, but is very sensitive to the high-rel military market.

10. Can you provide us with reliability test results of your product?

Motorola: No recent reliability test data available.

Raytheon: Do not have reliability data on standard process devices. They do not usually perform reliability testing.

RCA: Data has not been received at this time.

TI: They are not performing any routine reliability testing programs. They did perform extensive testing 3 or 4 years ago on discrete transistor beam lead devices involving a 6000-hour life test.

Users Surveyed

The following companies and government agencies were contacted to obtain information for this review. These contacts were selected because they are currently working with beam lead devices.

Sandia	- Albuquerque, New Mexico
Crane Naval Ammunition Depot	- Crane, Indiana
Bendix	- Kansas City, Missouri
Lockheed	- Sunnyvale, California
Raytheon	- Bedford, Mass.
Raytheon	- Quincy, Mass.

Sandia and Bendix have the greatest amount of accumulated beam lead experience in the industry, to date, with the exception of Bell Laboratories. They have about five years of experience on a broad cross-section of device types. The applications are ERDA (formerly AEC) and the Trident Program. Raytheon (Bedford, Mass.) has about five years of experience with complex beam lead IC's. Three years of this experience has been on SAM D ground systems.

Lockheed/NAD Crane have about two years experience with a broad cross-section of beam lead devices. This application is also for the Trident Program and is currently in the developmental stage.

Raytheon (Quincy, Mass.) has about three years of experience with beam lead devices. Their applications are in custom hybrid circuits.

These users were contacted and queried on a list of subjects by telecon. The summary of these conversations is provided rather than their response to each detailed question. This will provide better continuity to the information obtained.

User Survey Summary

Sandia: Several years ago Sandia made the decision to go predominantly beam lead. They are presently building a large number of hybrids which utilize beam lead discretes. Their experience has been good and they plan to continue the use of beam leads on future applications.

Sandia is using a wide cross-section of beam lead devices, generally high frequency types and, therefore, the devices have thin base regions and Vce maximums of about 30 volts. The Vce maximums result from the radiation hardness processing. They also are using all types of diodes, including zeners. The diodes cover the range from d.c. through microwave and includes pin, step recovery and Schottky barrier diodes. These devices represent both common types which were available in beam lead and types which Sandia paid for the development of the beam lead version of existing devices. They are not all available off-the-shelf, so they require procurement lead time. The majority of discretes

are purchased from TI and Raytheon and a few from Motorola. It would be possible to buy these using the existing Sandia specification, if desired.

It is estimated that they have used 6000 to 8000 devices per type for some 20 to 30 device types. They emphasize that the successful implementation of beam lead technology requires a strong commitment (technical and financial) in special handling and inspection procedures and the acquisition of production equipment. This is the approach used at Bendix (Kansas City), which is the manufacturing facility for Sandia.

Sandia has used beam leads for approximately five years. The decision was made then that standard chip-and-wire would no longer be used except where they were forced to. They still have some applications where chip-and-wire is used. MOS devices are not available in beam lead and their hybrid process is not designed for only the use of beam leads, like in the case of Bell Labs, which uses ceramic substrates with tantalum nitride resistors, etc.

The integrated circuits used by Sandia are all custom circuits with dielectric isolation, Schottky clamping, thin-film resistors and special hardening modifiers. These requirements have posed a problem for procurement. Integrated circuits are supplied by TI, Harris and RCA. The RCA product is being supplied in flat pack packages with beam lead die. Sandia is so convinced that beam leads are more reliable, they actually prefer packaged beam lead die over packaged chip-and-wire devices.

They have found, or developed, second sources for the majority of their devices. There are some cases where they have more than two sources. ERDA policy requires dual sources, where possible, so this has required development funding in some cases.

It is difficult to estimate delivery times because of the wide variations. Bendix has developed a list of projected times required for delivery. The best estimate would be 36 weeks for discretes and 50 weeks for integrated circuits. These times would include order lead-times

from start of manufacture through testing, screening and delivery. They feel these times would be comparable to chip-and-wire packaged devices.

They recommend a stringent front and backside die inspection which would be comparable to the requirements for a standard part to be used in a high-rel application. If electrical testing is performed on receipt (recommended by Sandia), then they must be purchased as an etched array; i.e., the die have been etch separated, but are held in wafer order by wax. In this configuration, the front side visual must be performed by the user. The wafer is attached to a sapphire slide with low temperature wax for etch separation and the slide is opaque. The inspection criteria should specifically address silicon nitride defects on the surface and cracks or missing silicon nitride at the nitride lip on the underside of the beam.

Sandia requires beam attachment integrity, beam hardness and sample bond testing on a periodic, or a 100% lot basis, depending on the supplier. These tests have been an effective screen. Sandia's bonding schedule requirements could be made available.

The electrical testing required is 100% d.c. probe at room temperature. They are working on a beam lead carrier which is about 80% complete. This would allow the elimination of the etched wafer array delivery requirement. Beam lead device procurement would be the same as for packaged parts. They do not foresee a problem with the carrier damaging the beam lead die, but do foresee a problem with obtaining high temperature operation. They are hoping for 125°C and are confident of 80°C. There is a large effort on carrier development by suppliers and users and the progress has been good.

For qualification testing, a sample is mounted in a convenient package, DIP or flat pack, and normally they are not sealed. Qualification tests are then performed as on a standard chip-and-wire packaged device.

They have not had any major beam lead problems. Very little screen testing has been done, to date, except the d.c. probe at 25°C. Prior to

d.c. probing, they perform a passive high temperature, 300°C, stabalization bake. This has been shown to be a good test for eliminating weak or marginal devices.

They have had very few beam lead bonding problems, however, one must first develop a good beam lead bonding process and then control it by sample destructive pull testing. They are using a chrome-gold substrate metal system. This requires a 450°C bonder probe temperature, so it is important to limit the holding time because of the Au-Si eutectic temperature of 385°C.

Sandia is using a thin-film Cr-Au substrate metal system. They have not used thick-film, to date, but they are studying it and it looks better now than it had earlier. Also, they have not used compliant beam bonding, but have done a lot of study work on it.

Their beam lead bond strength requirements are 1 gram-force per mil of beam width. This is an average and, therefore, could allow a weak bond to go undetected. Also, it does not apply to a large number of beams on a device; e.g., with a device with four beams five mils wide, the minimum pull force would be 20 grams; however, a device with 20 beams may have a minimum of 15 grams force. They recommended reviewing the study conducted by NAD Crane.

They have used coatings for die protection. They have looked at a large number of materials. They feel die protection is needed. Organic materials have been used, but have presented problems. A plasma deposited nitride is presently being evaluated. This coating is put down over the interconnect metallization. Its properties are not as good as the high-temperature nitride used to seal the surface, but they feel it is better than organic coatings. TI is developing the process and it is looking good. It is non-hermetic, but provides particle and scratch protection. TI is currently shipping it on their products. Sandia has not tried Parylenes. They have looked at this coating, but it is very difficult to rework. They do not build a hermetic sealed hybrid. They seal the hybrid package with epoxy and the leak rate is about 1×10^{-4} SCCS. Sandia has

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had no problems with moisture. They have had problems with conductive particles, but they are usually generated during rework.

They have found beam lead replacement to be reliable. Beam lead die have been replaced 2 or 3 times with no problems. This capability for rework is depended on very much for the economical repair and recovery of defective hybrid circuits.

Sandia has not observed any correlation to the experience reported by Hughes that the beam lead linear circuit failure rate was 2 to 1 over digital.

The future for beam lead applications at Sandia will continue to grow. Availability of complex custom beam lead product is a problem. Also, beam lead device selection is still limited by not including MOS or circuits which have trapped pads and cannot be beam leaded. Sandia has been forced to use chip-and-wire on the newer linear circuits because of the lack of a beam lead product.

NAD-Crane: Trident systems will use beam lead transistors and integrated circuits. They are presently trying to develop 13 integraded circuits which are similar to the TI 54LS series, except they are dielectrically isolated to provide radiation hardness. The device types include dual and quad gates, flip-flops, OP Amps, J-FET drivers, registor files, arithmetic logic units, ROMs, and RAMs.

The projected usage for simple gates are 1000 to 10,000 at the outside. More complex circuits would be 100 to 200 per year; 1 to 2 devices per system.

Lockheed began the beam lead integrated circuit development about two years ago. The degree of success has not met expectations. At this time it appears doubtful that all 13 device types will be developed.

Dual sources are being developed. There are three suppliers presently involved with the development program: Motorola, RCA and TI. Two of these three suppliers will be chosen (probably within six months) for production devices. The devices will be available from dual sources with equivalent mechanical and electrical parameters. Of the 13 types,

about 10 have been successfully produced. Out of these, 5 or 6 have had very low yields, less than one device/wafer. The yield for gates is in the 15 to 40% range. Reasonable yields are being obtained on devices with up to 16 beams, and yields are starting to increase on devices with up to 20 beams. For a 100 x 100 mil die, the metallization density is so great that it is difficult to achieve an acceptably low defect density. This is due to the beam lead process having twice as many process steps as conventional metallization.

There was no data on delivery time experience. It was indicated that the Lockheed developed product could be available through suppliers, but did not know on what time schedule, and Lockheed would have first priority. A reason for delay is that the Lockheed specifications are too tight for the current state-of-the-art. The radiation compensating diodes resulted in a larger die. This, and the dielectric isolation, are not compatible with the current specifications. Lockheed is working on relaxing the specifications, but they have not been finalized. Lockheed has a very tight visual inspection specification.

Electrical test is 100% d.c. probe. RCA has developed a die probe test capability which can perform d.c. and a.c. testing at 25°C and 125°C prior to wafer etch and separate. Lockheed has a 125°C spec requirement which presents a testing problem. The 125°C requirement has required the addition of temperature compensation components which further reduced wafer yields. After die separation, only sample electrical testing is done.

Lockheed requires beam attachment pull tests, beam hardness, and sample bonding tests. They also require an environmental test of packaged parts on a sample basis. They have not had enough experience to determine the effectiveness of these tests.

There is a spec requirement for 300°C HTRB testing. There are no carriers available which are capable of this temperature, so this test requirement is currently being waived. Development work is currently being funded for beam lead carriers. The development is incomplete at

this time. There is a good possibility of developing a carrier capable of 125°C, but it is questionable for higher temperatures. There has been a great deal of effort in this development, to date.

Beam lead device qualification testing is being performed by Lockheed. Beam lead devices are installed in flat packs for this testing. The qual testing is currently in progress, to a limited degree. They did not have any data on screen testing experience.

They have not had any major problem with beam lead bonding. An in-depth study has been conducted by NAD-Crane and the results will be reported at the 1975 ISHM Symposium. An advance copy of this report has been received from NAD-Crane. The study evaluated three beam lead bond strength test techniques. The techniques were push-off, pull-off, and blow-off tests. The results show the blow-off technique is no good and the pull-off technique is the best. The Lockheed bond spec is 1 gram-force/mil of beam width. This is not an optimum spec as it could allow an unbonded beam. It is recommended that a visual criteria also be required. Most of the breaks occur in the middle of the beam, if one beam pulls off or was not bonded it would be considered unacceptable. Visual inspection criteria has been found to be worthless for detecting marginal or unbonded beams. Bad bonds were purposely made, both by reducing the bonding temperature and by increasing the temperature. The bad bonds could not be detected from the good bonds.

Thin-film hybrid substrates are used with single-layer metal interconnects. The metal system is a tri-metal system (Ti, Pd, Au) on alumina substrates. For substrates requiring limited crossovers (30 or less), they will use a gold ribbon bond, and for substrates requiring a large number of crossovers (greater than 30), they will use an RCA microbridge crossover. This is a gold-plated beam with an air gap.

A protective die coating is a major problem. A moisture barrier is needed to prevent gold from deplating due to water condensation on the die surface. Bell Laboratories is using a coating that is placed on the die surface. The coating is transparent and allows visual examination of the die surface. The identification of the coating material in the process

used by Bell Labs is not known. Plans are to use a glass passivation on the die surface of the Trident devices. The glass should adhere to the surface if the silicon area is greater than the metalized area. The glass will not adhere to the gold metal and will probably crack so the class will only provide scratch and particulate protection and not moisture protection. A conformal coating will also be used over the substrates. Caution must be used because the coating expansion can cause beam bond lifts and coatings may impede hybrid circuit rework.

If high packaging density is not required (no size and weight constraints which demands beam lead), they recommend that chip-and-wire be used.

They could not comment on beam lead replacement reliability as no rework is performed at NAD-Crane. Lockheed is performing beam lead device replacement, but only prior to conformal coating of the substrates.

Reliability studies of beam lead devices have primarily been performed by Bell Labs. These studies relate to the Bell process and is not necessarily comparable to current supplier product reliability. They feel that the activation energy is the same for beam lead and chip-and-wire, and that beam lead may not be an improvement. They feel that the beam lead products currently being delivered have defects that would not be allowed by Bell Laboratories.

Bendix-Kansas City: Bendix is the manufacturing facility for ERDA and works in conjunction with Sandia. Bendix is currently manufacturing systems for ERDA and the Trident Program.

If certain precautions are taken with beam lead devices, the results can be excellent. When the device cannot be supplied in a carrier, it is recommended that the user perform; (1) electrical testing at the wafer level, and (2) wafer expansion (removal of the die from the etched wafer). Their experience has shown that the electrical yield will be significantly reduced due to damage during wafer expansion. The electrical fallout at the circuit level, for a digital integrated circuit, showed a 3-4% failure rate for devices which previously tested good by the supplier.

On discrete transistors, Bendix buys the etched wafer as tested by the supplier. They retest the wafer and compare results to suppliers data. If a reasonable agreement is found, the wafer is bought according to the supplier's count. If not, or if the devices have moved on the sapphire slide thereby invalidating further probe tests, these wafers are returned to the supplier.

In order to conduct the wafer expansion operation without damaging the devices, Bendix has purchased an automatic pick-and-place machine which is manufactured by Teledyne. This machine removes the individual devices which were tested good and orders them on another slide. The pick-and-place machine is automatically controlled from a punched paper tape which is generated during die probe. The etched wafer is placed on a heated stage to soften the wax. The pick-and-place machine removes and places the good devices in an expanded array on a glass slide for 100% front and backside visual inspection. Visual defects run about 10%. The devices are then picked up from this slide and bonded into the circuit with the wobble bonder. The big advantage of this method is that lead orientation is maintained and handling damage is held to a minimum. The cost of a manual pick-and-place machine is approximately $10,000 and an automatic machine costs $65,000. The manual system is acceptable for larger chips (75 mils and above). For the smaller chips, the automatic system is needed or increased damage will result during wafer expansion.

For integrated circuits, it is not desirable to buy non-expanded wafers, because the individual device costs are too high to discard the screened rejects. Therefore, a joint effort to develop Barnes-type carriers for beam lead devices was formed with Lockheed. The responsibility for the 029 series was Lockheed's and the 039 series was Bendix' (029 are 22 leads and less, while 039 are 24 leads and more). Suppliers worked on the development with Bendix and Lockheed. The 039 carrier contains a resilient pad to hold the device in place. This development is complete and this carrier will be used for integrated circuits procured on future programs. They feel that the wafer expansion is so important that they are supplying pick-and-place machines to TI and Harris for

their programs. These machines will be used to transfer the devices from the wafer and insert them into the carrier. This will allow the supplier to perform d.c. and a.c. parametric testing at high temperature and a complete front and backside visual inspection. The maximum carrier temperature is 175°C. Lockheed was striving for a 300°C temperature capability so that high temperature burn-in testing could be performed. At this point, it appears they may achieve 200-250°C. Bendix does not feel this temperature is required. They would like to have a carrier capable of 300°C, but the mechanical tolerances and thermal expansion coefficients cannot be controlled well enough. RCA is working on the development of a carrier using a glass plate, metal lands and a spring holding device. This may still present a problem for non-planar beam alignment. Their experience, to date, totalling over 5000 hybrids, has shown that burn-in testing at the hybrid level is not needed and has been eliminated. Burn-in testing of standard chip hybrid circuits is used primarily to screen bonding and leakage problems. These problems have not shown up in beam lead hybrids and apparently have been eliminated with the beam lead chip. Also, Bell Labs does not run burn-in testing on their beam lead hybrid circuits. The only high temperature screen Bendix performs on beam lead devices is a 300°C 16-hour stabilization bake at wafer level prior to separation etch. This has been found to be very effective in removing marginal and weak devices prior to installation.

Their experience with standard chip transistors, produced on their captive lines, and beam lead transistors provides an interesting comparison. Both configurations were tested, inspected and screened to high reliability criteria. The invested cost to the point of device installation in the circuit was estimated to be equal to or slightly lower for the beam lead devices. This estimate included the screen testing; i.e., burn-in, HTRB, hermetic seal, etc., required by the standard chip and electrical probe test, visual inspection and special handling required by the beam lead device. The point is that their experience has shown that even though handling, inspection and testing costs are higher for

beam leads, there are more screens and testing required by the standard chip device. The higher cost of beam lead devices over standard chips is mostly due to the lower production quantities of beam lead. However, a part of the higher costs is due to the increased complexity of the metal processing.

Their visual inspection specifications are similar to MIL-STD-883 requirements. The specification was not considered to be severe, but comparable to normal high reliability criteria. Bendix performs their own bondability tests using their substrates. They have not had much of a problem with bondability.

One problem to be aware of is stress induced cracking of the nitride during bonding. The cracking occurs at the nitride seal/beam interface. If this seal is damaged, the surface hermeticity is violated. Bendix has been working with TI to develop a stress relief point on the beam away from the nitride seal interface. The nitride cracking can be a problem during bonding if the bonder is not properly controlled.

A comment made by Teledyne, regarding bond operator training, was that it required 90 days of training for wire bonding and 3 days for beam lead bonding. This can be a significant cost item when one considers operator turnover and the effect of operator skill on the wire bonded devices.

Bendix is also currently buying three beam lead device types from RCA which are packaged in flat packs. The application circuit is under development and it is not certain whether the final configuration will require a printed circuit board or hybrid type of construction. Using this packaging approach will satisfy either type of construction. If the hybrid circuit is required, the beam lead devices will be ordered without the flat pack. This program is just getting underway so they have not developed much experience with these devices.

Their experienced assembly failure rate of .0065% is comparable to that reported by Bell Labs (.005%). The comparison to assembly failure rates using JAN-TX and MIL-STD-883-TXB devices showed a failure rate of

.036%. This represented a 14-month normal production interval and included 55,200 discrete transistors and 62,745 beam lead devices. This information is contained in a paper presented at the October 1975 ISHM Microelectronics Symposium.

Lockheed-Sunnyvale, California: Their beam lead experience began with the SAM-D and Safeguard Programs. They are currently working on the Trident Program which will use a broad cross-section of beam lead devices. Trident is the first program where Lockheed has used this level of beam lead device complexity. They are having some development problems with the complex circuits. They are currently reevaluating the complex memory devices with the possibility of using standard chip-and-wire devices.

A beam lead development program is in process to develop 13 custom integrated circuits with dielectric isolation (DI) for radiation hardness. There are many problems with the more complex devices, but the primary problem is related to the DI process. A high quality DI material is required and it has been difficult to obtain enough of this material. The material problems cause a serious impact on device yield.

They are using the Raytheon beam lead 741 operational amplifiers. This is a high-rel level part and has been delivered on time and performance, to date, has been good. They have had no problems with oscillation and the devices have met specifications. This is a standard product which is built on a highly controlled high reliability line. They are also using an RCA beam lead 741 OP Amp. This device has not had problems and they have been getting delivery.

They have had problems with OP Amps, but these were primarily with testing. The 741 has gone through several design changes over the past 2 years. The earlier designs would go into thermal latch-up, but there have been no problems with the later versions. The earlier problem was

related to the thermal placement of components on the die. This problem was not limited to the beam lead version. They have not had problems with offset at temperature on the 741, but this has been a problem on their custom linear development. The custom linear is a more complex circuit with special environmental requirements.

Their beam lead transistors are being supplied by TI. Program support has been good and there have been no significant problems.

They have used beam lead junction isolated 54LS191 counters on another program and have not had significant problems. These devices have been bought in 500-1000 piece quantities.

The majority of the problems have been with assembly, test and conformal coating over the beam lead devices. It has been difficult to obtain a coating which covers well, holds moisture (so it does not condense out on the die surface) and allows reasonable repairability. They feel the conformal coating is necessary and would use it in a hermetic package for conductive particle protection. The coating is intended to absorb moisture and keep the moisture molecularly bound without swelling of the coating. All silicones do this to some degree. Bell Labs is also using a conformal coating, but they do no rework once the circuit is coated. Lockheed is trying to develop a method of reworking after coating by using a stripper to remove the coating. The stripper causes the coating to swell and lifts beam lead bonds. At this time, it does not appear that repair after coating is compatible with the problems of coating removal. The coating also must be compatible with solvents used to clean the hybrid substrates.

Each supplier's processing is different. They feel TI is the closest to Bell Labs processing. Some examples of the differences are: method of emitter metallization contact, if an oversized mask is used; if two masks are used to open a contact through nitride and oxide; or if nitride is used as a mask for underlying oxide. These are primarily reliability concerns rather than electrical concers. The product available to the military high-rel user is not comparable to the Bell Labs product.

If one could use the Bell Labs/Western Electric product, one would have few problems. Bell Labs/Western Electric is shipping approximately 30 million beam lead devices per year. With that volume, the problems get solved. Bell Labs has addressed and solved problems which everyone else is just beginning to experience. They are probably 5 years ahead of the industry. The semiconductor industry has not pushed the beam lead technology, so it has not yet experienced all of the problems. With Lockheed's investment in beam leads, they have a commitment to use them in future programs.

The reason for utilizing beam leads was that program size and weight constraints required hybrid circuits. Beam leads were preferred over chip-and-wire as they would eliminate flying leads, epoxy die attach, and dependence on hermetic hybrid package seals. They also wanted to use a monometallic, thin-film, precious metal system. It also was felt that beam leads would provide an improvement in system reliability. Without the need for hybrids, the need for beam leads probably would not exist.

The requirements for high temperature beam lead device screening; i.e., burn-in, HTRB and limited life test, has not been fully established. It appears that the ability to run a full temperature screen on operational amplifiers for example, would provide a much improved part. Screening would not be that necessary for digital devices. Also, previous experience shows that more in-depth testing is a smart thing to do for an immature technology. If the technology were mature, as the Bell Labs product, it would be a waste of money to perform high temperature screening. They would like to have the capability available, but the program does not require it. They are hoping to have a high temperature carrier for all part types, but especially for the linear circuits.

Beam lead device qualification testing has not started. They are currently performing device evaluation testing which is similar to an engineering device evaluation. Part of this testing is to evaluate a powered high temperature (250-300^{o}C) accelerated life test and answer

two questions; (1) would the test be effective in removing infant mortality? and (2) would it significantly subtract from the total life of the part? The answers are; (1) yes, it does effectively screen out early failures, and (2) no, it did not significantly subtract from total operational life times. It was compared to dynamic burn-in and lower temperature burn-in and the results were that powered high temperature accelerated life test was more effective. These tests have been conducted on transistors and digital circuits, to date.

They have done beam lead reliability testing and at this point in the program they feel the comparison of reliability between beam lead and chip-and-wire is even. As the beam lead process matures the reliability will increase. One of the more significant problems they have realized is the degree of complexity that can be constructed on a hybrid substrate and the difficulty it presents in testing. Therefore, they recommend limiting the number of devices per substrate to 10 and definitely not over 20 with devices such as counters, shift resistors, etc. (complex SSI to low MSI). The greater the quantity of chips, the higher the probability of rework. Rework is not a problem, but failure diagnosis and fault isolation can be a big problem. It is very difficult and time consuming even when automated fault isolation is used. Also, this is not available for analog circuits. In their hybrids, they are using beam lead chip resistors. Initially, these provided some unexpected problems. It is fact that failure diagnosis and fault isolation will become a major production throughput problem. This has been stated many times, but nothing makes you realize how true it is until you experience it. Also, Bell Labs has found that when you are designing a new level of circuit complexity, you should include fixed point probe lands on the substrate metal pattern. These lands should be located to provide stragetic circuit node voltage points for use in circuit fault isolation. The need for lands is dependent upon the circuit complexity and the difficulty in obtaining quick fault isolation. And the easier fault isolation can be accomplished, the lower the product cost. The land

should be dimensioned to be compatible with the mechanical positioning accuracy of the probe system used. Five to six of these lands per substrate can be invaluable.

In their application, they will use a non-hermetic hybrid with a conformal coating over the circuit. There are a number of tradeoffs to be made between a hermetic and non-hermetic package. For example, the feasibility of rework after package seal, detection of package seal leaks, package costs and conductive particulate protection. Bell Labs uses a silicone conformal coating over their circuits and they would like Western Electric to implement a low temperature plasma deposited nitride coating on the chip surface. They understand that Bell Labs is not using a conformal coating on the chip surface only. TI is currently shipping beam leads with the plasma deposited nitride on the chip surface. (Note: This coating should not be confused with the pyrolytically deposited nitride which provides the hermetic seal for the chip surface.) This coating is transparent and does not present a problem to visual inspection of the chip surface. The coating is intended primarily for particle and mechanical protection of the metallization and chip surface. It may also provide some moisture protection as well. Lockheed has not seen any cracking or crazing of the coating, but their experience is limited as it is a new process.

If the industry does not utilize and market beam lead technology, it is doubtful if any further improvement in reliability can be realized. Beam lead utilization by the high-rel industry will probably increase with the availability of carriers. However, product availability also needs improvement. There would be no hesitation to committing to hybrids using beam lead transistors as they have had very few problems with them. However, one of the largest problems with digital integrated circuits is there has never been much production generated. Actually the linears have had larger quantities produced.

Raytheon-Bedford, Mass.: Their experience in beam leads has, for the most part, involved one complex array. For the last five years they

have been using a 60 gate array in digital processing equipment in SAM-D ground systems. This array is fabricated in the Raytheon-Bedford facility and the Raytheon Semiconductor-Mountain View facility. It has also been manufactured in limited quantities by TI and Motorola. Four to six arrays are installed in a RAYPAK which is a non-hermetic polymer sealed package. The performance has been very good. The problems have been related to the functional testing of multiple complex arrays, rather than with problems of beam lead device failures, beam lead bonding, packaging or thick-film hybrid problems.

The 60 gate MSI array has 50 beams and is a high-rel level device which is manufactured under specific controls and visual inspection criteria. Lot samples are used for electrical and mechanical evaluation prior to lot acceptance. There is no device electrical screening beyond the 100% d.c. probe at room temperature. Their basic philosophy is like Sandia/Bendix where an in-depth d.c. electrical probe is used in conjunction with a sample for lot evaluation and qualification. This approach has been found to be very satisfactory. With the implementation of thorough visual inspection and control of the beam bonding process, they have begun to realize the reliability potential of beam lead devices and are approaching the reliability that has been reported by Bell Labs and others.

One of the negative aspects of beam leads is the inability to purchase the less common discrete devices quickly. When the SAM-D Program began, 3 years ago, they were told that most any type of device was available in beam lead. This was not true then and it is not true now. Many times it was, and is, necessary to work around this non-availability and perturbate the parts list for design. To start today, you must first have an accurate knowledge of what devices are available in beam lead and establish a strong parts program which does not allow utilization of parts which are not available in beam lead. From an application standpoint, be careful of availability. From a reliability standpoint, the technology is everything it is reported to be.

They have not experienced electrolytic conduction due to condensation as reported by Hughes. They use a polymer sealed package and, on engineering test units, have coated beam lead devices on substrates with a urethane type of conformal coating. They have had no problem with moisture. The coating was used for protection against mechanical damage during handling. Actually, one may be better off without coatings as they sometimes entrap moisture.

It is their feeling that the product available from suppliers is close to Bell Labs product. The performance experienced by the users of beam lead devices would support Raytheon's feeling about their devices.

It would be helpful if suppliers would maintain a large available stock of beam lead devices. This would help to interest additional users if devices were known to be available. ECOM (Army-Fort Monmouth) will, as a part of their contract with Motorola, develop a stock of about 50,000 devices for 35 part types in hopes of developing further use of beam lead. They feel that the visual inspection requirements can best be described by Bendix.

Raytheon is using a thick-film conductor on their hybrid substrates. Thick-film is lower in cost as compared to thin-film and an advantage they have found is that the beam lead bonding process is more easily controlled for thick-film. Bonding problems, which have been experienced with thin-film; i.e., hardness of substrate gold, surface condition, and beam hardness, are not a problem with thick-film. They have not had beams lift off after bonding. The MSI device that Raytheon is using has 50 beam leads and is the most complex device being production bonded. The majority of their experience is in the complex devices. The 60 gate array has accumulated about 3×10^7 hours with 2 electrical device failures.

They had compiled data from qualification and lot testing for simple digital gates, test vehicles and 60 gate arrays. A copy was provided for review. This data included the 883 Level B qualification test program and performance, and lot by lot screen test plan and performances.

The calculated failure rate compiled from the lot screening data is 0.17 failures/10^6 hours (parametric) and 0.06 failures/10^6 hours (functional). Also, evaluation test results of beam lead module assembly showed the "experienced" beam lead bond failure rate was less than .03 failures per 1000 bonds.

Raytheon-Quincy, Mass.: They are a custom hybrid circuit manufacturer. About three years ago, two customers asked that beam lead devices be used where possible in their hybrid circuits. The purpose was to eliminate wire bonds, gain a monometallic interconnect system and thereby realize improved reliability. These circuits represented two levels of complexity: one contained about 25 integrated circuits and the second contained 6 diode and transistor devices.

The first problem encountered was that beam lead devices were not readily available. This necessitated two hybrid layout designs; one for beam lead and one for standard chips. During the first year it was necessary to switch back and forth depending on beam lead device availability. Based on this experience, a paper was presented at the May 1975 Electronic Components Conference. This paper makes a comparison, based on their experience, between beam lead and standard circuits. The comparison considers the requirements for each technology from device procurement through hybrid manufacture. The basic finding reported was that the beam lead product achieved higher yields than chip-and-wire. The paper considers the cost and yield tradeoffs, but does not address the reliability tradeoff. The comparisons are made on a subjective basis, but the information could be helpful to others making a similar evaluation. One advantage claimed for chip-and-wire is the non-destructive pull test for wire bonds. The availability of beam lead devices continues to be a very limiting application consideration. They have experienced instances when a sole source supplier could not produce a device and this has resulted in complete shutdown of their hybrid circuit production. When these problems occur, one has second thoughts about new beam lead applications. As the technology stands today, beam

lead devices are more expensive than standard chips, therefore, device suppliers are not using them in their packaged devices. Until the demand for beam lead develops to increase the production levels and improve availability, beam leads will continue to experience problems of cost and availability.

An estimate of the differences in the two technology reliabilities could not be provided due to limited field experience. There has not been enough time accumulated to develop a comparison. If the two technologies are manufactured under high reliability controls, both will give very reliable performance. Therefore, to resolve any technological reliability differences, a large number of circuits and operating hours are required.

Raytheon-Quincy supplies hybrid circuits primarily for military applications and, therefore, only utilizes hermetic sealed packages. All of their experience has been with digital circuitry.

They had tried to use an overcoat on simple circuits, but experienced a great deal of difficulty. The coatings absorbed or trapped solvents during circuit cleaning and the coating produced strain on the beams which resulted in open and intermittent bonds at the die and substrate interfaces. They were unable to find a coating material which would solve these problems so circuit coating was eliminated. Beam lead devices are easily damaged when mounted on an exposed substrate. They cannot withstand the usual handling forces and must be protected. This was instrumental in the development of their RAYPAK which provides a protective enclosure for beam lead devices.

They feel the future for beam lead devices is still questionable and that it could go either way. The development support being provided through the Trident Program has done a great deal to keep the beam lead technology going.

User Survey Summary

There currently is a fair number of applications which are utilizing beam lead devices and the experience relates a respectable level of

performance. Although a relatively young technology, it is reported to be measuring up well with standard chip-and-wire devices. Due to its immaturity it has 3 major factors which are holding back wider acceptance.

The first factor is availability. The availability of beam lead devices, both part type selection and available stock, have presented major problems to the hybrid circuit manufacturers. This problem reduces down to a problem of supply and demand. Until the demand increases, the supply will be limited and slow, and the demand will not improve until beam lead satisfies needs of the hybrid circuit manufacturers who are not satisfied by the standard chip-and-wire technology. When beam leads first became a reality, standard chips were suffering from a number of reliability problems. These problems have been solved, or relieved, such that in the majority of applications reliable performance has been realized.

The second factor is that a satisfactory high-temperature carrier has not yet been developed and the chips can only be d.c. electrically tested at ambient temperature. D.c. and a.c. testing over full temperature is one of the advantages to be offered by beam leads once the carriers are developed. With the availability of beam lead carriers, complete electrical tests over the full temperature range will provide a significant parametric test and reliability advantage over standard chips. Carriers should be available for most devices by early 1976. High temperature (greater than 200^{o}C) operating capability for carriers is questionable at this time.

The third major factor is the problem of the coating needed to provide adequate device surface and mechanical protection. The device needs to be protected from conductive particulate shorts and from mechanical damage which may occur during handling or in service. The gold conductor electrolysis problem found by Hughes in their evaluation has not been experienced in any applications, and the evaluation parameters appear much more severe than would be realized in actual applications. Development and application evaluation is in progress for various protective coating methods. The results, to date, have been very encouraging.

The majority of the industries experience with beam leads has been with applications of discrete devices. Many of the integrated circuit types in use employ dielectric isolation for radiation hardness. Dual sources are usually available for current device types.

Delivery times have been found to vary widely. The typical time required from the time of order to the time of delivery for a military level device is 40 to 50 weeks. Many devices are produced on an as needed basis. However, the delivery times are comparable to standard chip devices which have requirements for special lot controls and inspection requirements.

Thorough front and back visual inspections are necessary for reliable performance. Qualification and sample screening tests can presently be accomplished without carriers through the use of uncapped flat packs or dual-in-line packages.

The majority of hybrid substrate systems being used for beam leads are thin-film. Thick-film experience with beam lead looks promising and could begin to find more usage. Thorough beam bonding process and control criteria must be developed and implemented. Bond reliability is dependent on process control as post-bond visual inspection cannot detect weak or unbonded beams. Destructive bond strength evaluation is best accomplished by a device pull-off test. Acceptability should be determined by a pull force minimum with visual criteria identifying failure mode limits.

The survey consensus was that a beam lead die coating is needed. The requirement for a coating and the specific type must be determined by application and tradeoff considerations. Silicone coatings have primarily been used, to date.

Beam lead circuit repair has been reliable, but it must be accomplished prior to conformal coating when it is used.

Electrical testing and failure isolation can be a big problem with complex hybrid circuits. This problem can be reduced by limiting circuit complexity and including substrate circuit test lands.

Hermetic packaging of beam lead hybrid circuits is not required, but mechanical protection of the beam lead devices must be provided. The devices are easily damaged during routine handling.

Beam lead circuit reliability was reported to be equal to or better than chip-and-wire. Performance data has shown a significantly lower failure rate for beam lead devices as compared with high-rel discretes.

Recommendations and Guidelines

1. In designing hybrid circuitry, beam lead devices should not be selected solely on the basis of information in the part manufacturer's catalog. The beam lead parts listed in a manufacturer's catalog as "available" are probably a combination of parts ranging from a few parts in current high volume production, to parts where masks exist, but no parts have been yet produced, to many parts for which no production is planned until 1976, or later.
2. Because of the above problem, the exact production status of each contemplated beam lead device should be determined prior to placing the part on the program parts list.
3. Parts which are listed in catalogs, but have never been produced, should be regarded as high risk items from the standpoints of both availability and reliability, since there is no assurance that serious processing problems will not be encountered when production is initiated.
4. Because of the problems described in the preceding paragraphs, the part specialists, not the electronic circuit designers, should control the selection of the beam leads to be used.
5. In selecting beam lead parts, it should be recognized that a dielectric-isolated part in current production, although more expensive, may be a better cost/reliability risk than initiating the development of an initially cheaper non-dielectric part. (This guideline applicable where there is no requirement for radiation hardening.)

6. Consider performing DPA (Destructive Physical Analysis) as a means of baselining the initial procurement, with subsequent DPA's, to monitor the quality of subsequent procurements.
7. In program planning, a delivery time of about 12 months should be planned for high reliability products. For standard, off-the-shelf products, delivery times vary from 1 to 4 months.
8. A successful beam lead program requires a serious and substantial commitment of resources. The following items are listed to roughly scope this overall task and to give the reader an impression of the scope of the commitment to be made. These items also could be used as a checklist for use in design reviews.

Parts Specification Development Effort

- Identify beam lead device front and backside inspection requirements.
- Identify sample inspection criteria; i.e., nitride quality tests, beam quality tests, etc.
- Identify electrical and environmental test requirements (determine carrier availability).
- Identify screening and/or qualification test requirements (include sample size and vehicle for test, carrier or package).
- Identify packaging method for shipment (consider device protection, visual inspection and electrical test at point of receiving).
- Coordinate specification requirements with supplier(s).

User Process and Inspection Development Effort

- Develop receiving procedures for handling, inspection and electrical test. (Devices are fragile and present a new step in miniaturization.)
- Identify the hybrid substrate process technology. Consider tradeoffs and previous industry experience.

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- Develop detailed beam lead device bonding criteria (matrix substrates and cross-section of beam lead devices). Evaluate beam bond strength, bonder parameters, post-bond temperature anneal, beam lead device damage, and bonder performance stability.
- Determine beam bond strength test method and criteria, sampling plan for production beam strength verification and post-beam bond visual inspection criteria (nitride damage).
- Identify hybrid package and substrate coating requirements. Evaluate the proposed method and verify compatibility with system requirements. Determine if adequate protection is provided to the circuit and that coatings do not create unacceptable risks.
- Develop beam lead circuit repair philosophy and device replacement procedure. To what point in production can device replacement be performed, how defective device is removed, substrate land preparation and device rebond procedures, identify re-inspection requirements.
- Develop criteria for limiting hybrid circuit complexity to a testable level. Consider failure diagnosis and failure isolation methods and time requirements. Consider the use of substrate circuit lands for reducing failure diagnosis and failure isolation times.

Acknowledgement

This writer would like to express his gratitude to those individuals and their companies and centers for their time and participation in this review. It speaks well for their interest in beam lead technology and their desire to help in its continued progress. Without their participation this review would not have been possible.

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APPENDIX F

WET SLUG TANTALUM CAPACITOR STUDY

TANTALUM CAPACITOR STUDY

The Avionics Laboratory's statement-of-work to Autonetics specifies that tantalum capacitors should be the solid type and, thereby, prohibits the use of the wet slug tantalum capacitor. This is a well-founded and excellent guideline based on past bad experiences with wet slugs. Unfortunately, the penalty paid for the much larger volume and weight of the dry capacitor sometimes, and in fact, frequently forces the reluctant abandonment of this reliability oriented rule. For example, on both the Viking Program and the Space Shuttle Program, valiant attempts to outlaw wet slug capacitors were in the end unsuccessful because of the severe weight and volume penalties.

The two problems encountered with wet slug tantalum capacitors are; 1) leakage of sulphuric acid, which is catastrophic to the surrounding electronics, and 2) migration of silver from the silver case to the tantalum slug, causing degraded performance, failure, and sometimes an explosion of the capacitor. The problem of leakage has been solved in recent years with the development of reliable hermetic seals, thus, the remaining concern is silver migration. This problem could be obviated if the case of the capacitor was also constructed of tantalum, rather than silver. Two such developments exist; 1) Leon Hamiter of NASA's Marshall Space Flight Center is working with Sprague on the development of an all-tantalum capacitor, and 2) Plessey Electro-Products Company of England developed such a capacitor 12 years ago, which has been used in England and is currently being qualified to U.S. Military specifications. Autonetics is currently investigating the Plessey capacitor for possible application in MICRON. In the event that Autonetics determines the Plessey and the Sprague capacitors are unacceptable for MICRON, because of application, technical or immaturity problems, then the possible use of the conventional wet slug tantalum capacitor may have to be addressed. It is with this possibility in mind that we prepared guidelines for the <u>successful</u> use of wet slug capacitors. Because of concern on the Viking Program, Martin Marietta conducted an exhaustive test program to fully assess the problem of silver migration. These test reports have been sent to Autonetics, but they do not contain specific guidelines. Therefore, in conjunction with the authors of this data, the following guidelines were developed which, if followed, will guarantee that silver migration problems will not occur.

The Viking wet slug tantalum capacitor test program demonstrated conclusively that this type of part performs reliably at or below the following environmental and circuit application levels:

1. One thousand hours of non-sinusoidal (i.e., square wave and modified sawtooth) ripple currents as high as 350

milliamps and 270 milliamps rms, respectively, for case size GT-3 General Electric capacitors, at frequencies as high as 72 KHz and at an operating temperature as high as +70°C or as low as -37°C. Some parts were operated with an applied d.c. bias as high as 66% of rated voltage or as low as 20%.

2. One hundred eighty-hour total temperature soak at 125°C is a static (non-operating) state.

3. Sine vibration levels of 50g from 10 to 2000 Hz.

4. Random vibration of 25g rms in two axes.

At logarithmic time points during the ripple current test program, randomly selected test specimens were micro-sectioned and submitted to chemical and microscopic visual analysis. Additional parts were evaluated in a similar manner at the completion of the test program. No evidence of silver migration, or other deleterious effects, were observed in the examined specimens other than normal characteristics. If anything, the test groups were in better condition than the control group with fewer and/or small silver flowers and with an improved silver-in-the-electrolyte condition. The tests helped prove that the worst possible thing to do to a WST capacitor is to leave it sit on the shelf for a long period of time; such as 3 to 5 years, thus allowing silver to go into solution in the sulphuric acid. The silver in the electrolyte immediately is plated back out on the silver case when the capacitor is operated, but no single non-operating exposure should exceed several years.

WST Capacitor Application Criteria

1. At moderate and higher vibration levels (i.e., up to the levels mentioned previously), use a second crimp near the base of the case to force the internal spider to grip the tantalum slug more tightly. This will prevent the slug from moving during shock or vibration and will, therefore, prevent the scuffing of the thin oxide coating due to movement of the slug against the spider. Preventing damage to the oxide coating on the slug will prevent the typical increase in leakage current (with a resultant decrease in maximum allowable working voltage) normally associated with shock and/or vibration effects.

2. If the part is to be used at high temperatures, a slightly greater case thickness should be used to permit withstanding the higher internal pressures without case deformation (bulging).

3. The capacitor case should be securely bonded to the PC board or other supporting structure.

4. Connecting leads must be stress relieved.

5. The hermetically sealed MIL-39006 series part is superior.

6. Use an oscilloscope with a clamp-on current probe to measure ripple current amplitude and waveform in each capacitor in a breadboard circuit. Be sure the application is bracketed by the Viking test data.

7. Take positive steps to prevent any application of reverse voltage to WST capacitors as follows:

   a. By analysis and test ensure that no sneak circuit exists that will allow a reverse voltage to reach a WST capacitor.

   b. Physically remove and use large posters to ban high power multimeters (e.g., Simpson 360, Triplett 630, etc.) from any area where WST capacitors are used in circuits and/or where troubleshooting may take place. An HP-427A or Simpson 2795 meter is considered safe on low-ohm ranges only (x 1 and x 10).

To further emphasize the degrading effects of even very small reverse bias voltages, the following case history from the Viking Program is presented. During the Viking Program all the electronic design engineers were directed to thoroughly analyze their circuits to be certain that no reverse bias from sneak circuits, or from any cause, could ever be applied to the capacitors. After this design review was completed and all identified problems reported were corrected, a WST capacitor in the Soil Sampler Control Assembly (SSCA) exploded, almost completely destroying the hardware. What had happened was that when the Viking Lander was unpowered, but connected to the power-up ground equipment for a long period, an undetected sneak circuit existed which placed a small reverse bias on the WST capacitor in the SSCA. Although this bias was only 0.250 volts, it was sufficient to grow a silver bridge between the silver case and the tantalum slug, causing an electrical short within the capacitor. When power was finally applied to the Viking Lander, the capacitor exploded. This is the reason that most multimeters must be purged from areas where troubleshooting activities may occur. It should be mentioned that in practice this is difficult to do. For example, when Martin engineers were visiting one Viking subcontractor, the lab foreman assured them that he had purged

his area of all Simpson 360's. Yet, when he opened his desk drawer, there was a Simpson 360. A Simpson 360 is an excellent instrument and he was simply unwilling to give his up. To put this experience in the proper context of the MICRON Program, it should be mentioned that the one billion dollar Viking Program involves only two spacecraft, no mission failures are permissible. In the case of the MICRON, a repairable aircraft device, a somewhat lesser emphasis on the prevention of reverse bias problems is probably appropriate.

In summary, WST capacitors are good reliable parts if properly applied. Neither high nor low frequency ripple current is degrading, provided sufficient d.c. bias exists to prevent polarity reversal during the negative half cycle of ripple current. However, these parts are very, very unforgiving of reverse bias, whether applied in a circuit or from troubleshooting with an ohmmeter.

Mr. Holtz participated in several meetings regarding wet slug tantalum capacitors and the silver migration problem. At one of the meetings, a presentation was made by Mr. Martin Mintz, Manager of tantalum products for Plessey Electro-Products in Los Angeles. He presented technical details of a wet slug tantalum capacitor that would positively not have the silver migration problem because it is totally all tantalum with no silver involved in the physical make-up. This capacitor has been used in England for 12 years and is presently in the process of being qualified as an ER part in the United States under MIL-C-83500 and MIL-C-39006. Also, Mr. Holtz presented to Autonetics' parts engineers reports from the involved technical study of wet slug tantalum capacitors described above.

APPENDIX G

COST-OF-OWNERSHIP TRADE OFF STUDY OF TEMPERATURE CYCLING ACCEPTANCE TESTING OF MICRON

COST-OF-OWNERSHIP TRADEOFF STUDY OF TEMPERATURE CYCLING ACCEPTANCE TESTING OF MICRON

Background

The specification on Reliability Demonstration Testing, MIL-STD-781B, contains an option to subject the equipment to a preliminary debugging (burn-in) period to eliminate a major portion of the infant mortality. This testing was tentatively defined in our Reliability Demonstration Plan, MCR-74-357, as eight temperature cycles plus vibration. This testing would be conducted just prior to the formal Reliability Demonstration Test and would also be subsequently conducted on each MICRON production article as a MICRON production acceptance test.

Purpose of this Study

The purpose of this study is threefold:

1. To establish whether eight cycles is the most cost-effective number for the specific case of MICRON.

2. To estimate the overall cost savings to the government thus substantiating the need for a stringent acceptance test program.

3. To establish whether continuous monitoring during the test is cost-effective as compared with monitoring only the first and last temperature cycles.

History of Temperature Cycling Acceptance Testing

An industry survey was conducted under Contract NAS9-12359 in 1972. It was found that the practices of the 26 companies surveyed were widely variable, varying from one to 25 cycles, as shown in Table 1. This uncertainty was resolved by acquiring discrete failure data from seven companies. This data showed that the desired number of temperature cycles was in the range of six to 10, as shown in Table 2 and Figure 1. This data, plotted in different formats, is shown in Figures 2 and 3. After the completion of NAS9-12359, the Air Force (SAMSO) and Lockheed used these findings to establish a requirement of eight cycles which, in 1974, was specified in their MIL-STD-1540. This specification defines testing for spacecraft hardware.

The foregoing background history was the basis for establishing the value of eight in our preliminary MICRON Reliability Demonstration Plan, MCR-74-357, and this study is being performed to support the finalization of this plan.

TABLE 1

Summary of Recommended Temperature Cycles From Industry Survey*

Supplier/Agency	No. of Cycles Recommended	Temperature Employed (°F)	Temp. Range (°F)
Lockheed Missiles and Space Co.	8 to 10	-20 to 160	180
General Electric Co.	6 to 10	-65 to 131	196
Aerospace Corporation	6 to 8	Variable	-
Decca Radar, Ltd.	20	5 to 131	126
Radiation, Incorporated	10 to 25	-65 to 131	196
TRW Systems	8	Variable	-
Martin Marietta Aerospace	6 to 10	Variable	-
Boeing	3 to 12	-65 to 131	196
Hughes	Variable	Variable	-
Motorola	22	-65 to 160	225
Collins Radio Co.	9 to 25	-65 to 160	225
Honeywell, Incorporated (Denver)	12	-13 to 131	144
Hewlett Packard Co.	16	32 to 131	99
Grumman Aircraft Engineering Co.	4 to 6	Variable	-
Bendix Corporation	6	Variable	-
Delco (AC) Electronics	5	-20 to 120	140
Raytheon - Equipment Division	5	32 to 160	128
RCA	3**	Variable	-
Westinghouse	3 or 4	Variable	-
Sandia Corporation	3 to 5	-65 to 160	225
Texas Instruments	2 to 10	-67 to 131	198
Barnes Engineering Co.	2 or more	Variable	-
Goddard Space Flight Center	1**	Variable	-
JPL	?**	Variable	-
Supplier A	5	-65 to 131	196
Supplier B	1	-65 to 165	230

* These are the opinions of the individuals consulted. They may or may not represent the current practice of the referenced companies.

** Additional cycles are required at the subsystem/system level thermal-vacuum tests.

TABLE 2

Companies Supplying Failure Rate Versus Temperature Cycle Data

Company	Type and Size of Data Sample	Were Hi-Rel Parts Used?	Was Vibration a Part of the Cycle?	Temperatures Employed
General Electric	80 Radar Systems	Yes	No	-65°F to 131°F
Lockheed	80 Command Control Systems	Yes	No	Variable - Most temperature differentials were 160°F
Boeing	150 SRAM Systems	Yes	Yes (2g)	-65°F to 131°F
Collins Radio	360 Radios	No	Yes (2g)	-65°F to 131°F
Decca Radar	10 Radar Systems	No	No	5°F to 131°F
Motorola	270 Radar Augmenters	No	Yes (2g)	-65°F to 160°F
Aerospace	21 Transponders	Yes	Yes	Unknown

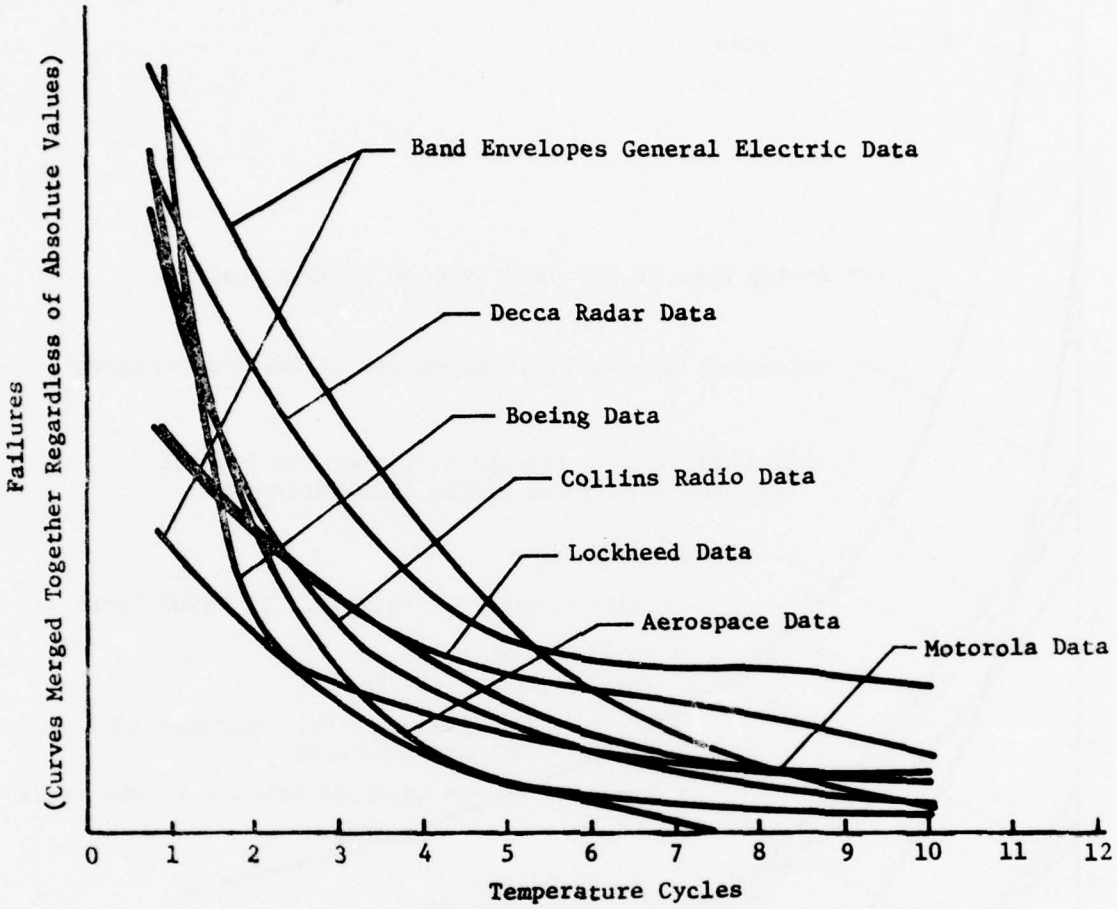

Figure 1 Summary of Industry Survey Data Indicating Six to Ten Cycles Are Required for Elimination of Incident Defects

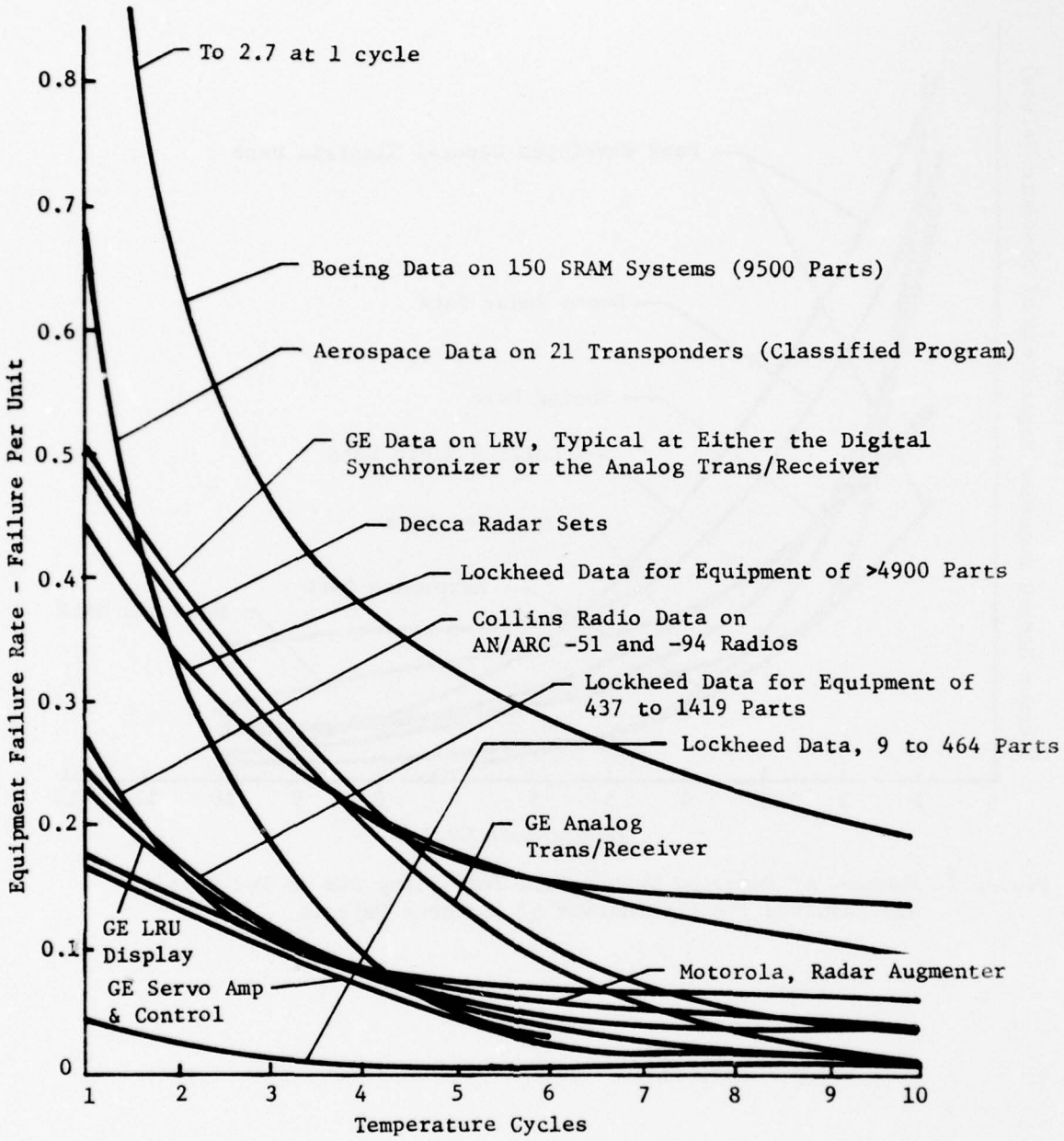

Figure 2 Summary of Industry Failure Rate Data

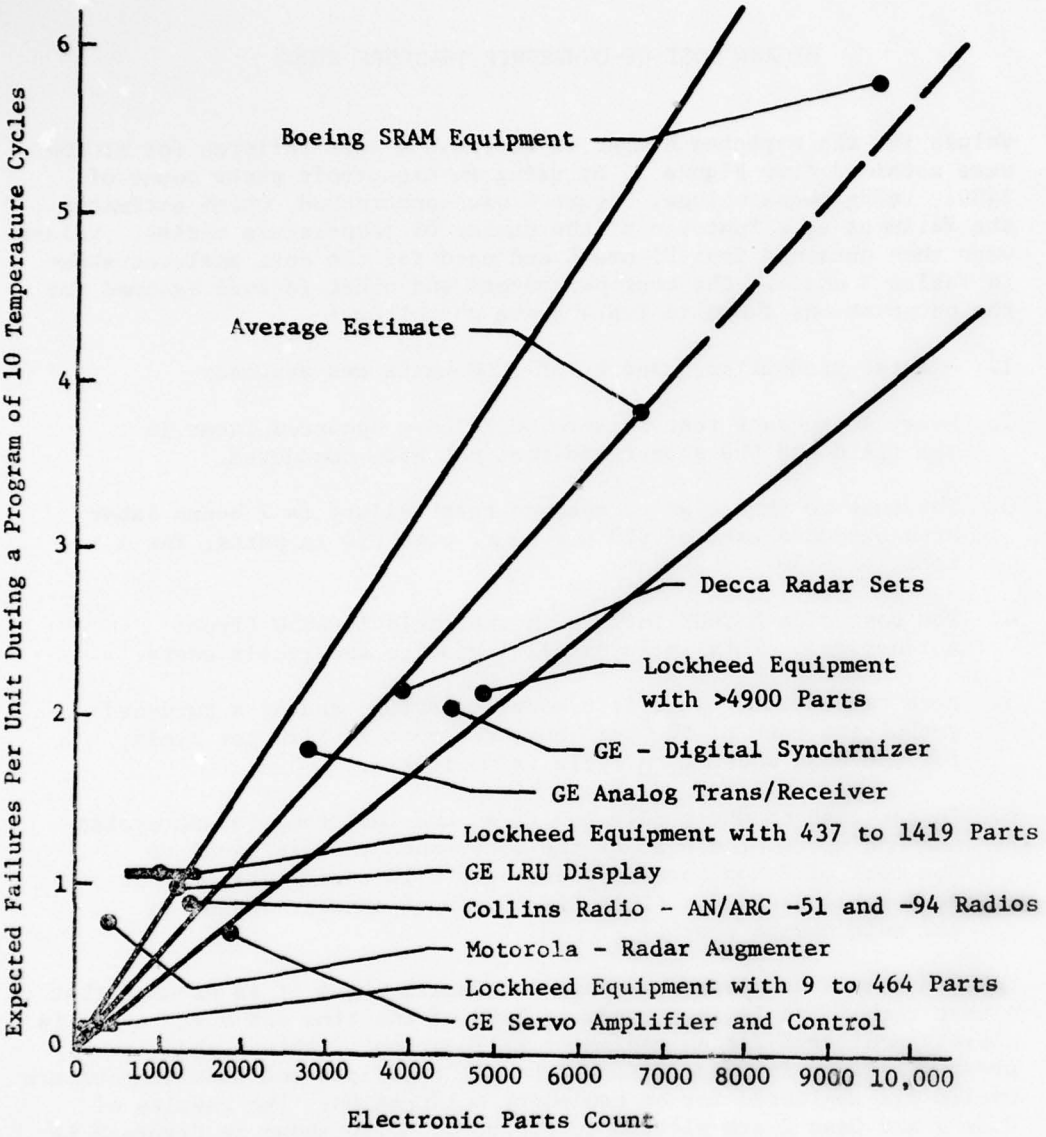

Figure 3 Expected Failures During Ten Temperature Cycles as a Function of Equipment Complexity

MICRON COST-OF-OWNERSHIP TRADEOFF STUDY

Values for the expected number of acceptance test failures for MICRON were obtained from Figure 3, by using an electronic parts count of 2400. Using these values, Figure 4 was constructed, which estimates the failures as a function of the number of temperature cycles. Values were then obtained from Figure 4 and used for the cost analyses shown in Tables 3 and 4. The cost parameters and other factors assumed for the computations shown in Table 3 are as follows:

1. A total production quantity of 1000 units was assumed.

2. Every acceptance test failure would have occurred later in the field had the acceptance test not been conducted.

3. The cost to repair an acceptance test failure is 7 hours labor at a burdened rate of $20 per hour, plus $10 in parts, for a total of $150

4. The cost of a MICRON failure in the field is $850 (from Autonetics). This includes all logistics and repair costs.

5. Each temperature cycle is 6 hours duration, and at a burdened technician rate of $20 per hour, the cost is $120 per cycle, for the case where <u>each</u> cycle is monitored.

6. In the case of where only the first and last temperature cycles are monitored, the cost of the acceptance test is equal to the cost of 2 monitored cycles, plus a 1% cost increment for each cycle above 2. (This takes care of chamber operation and maintenance costs.)

Table 3 shows the program savings for Case 1 where it is assumed that a test technician is in attendance 100% of the time and every cycle is closely monitored for an equipment malfunction. Table 4 shows the program savings for Case 2 in which only the first and last temperature cycles are monitored for an equipment malfunction. The results of Case 1 and Case 2 are plotted in Figure 5. Also shown in Figure 5 is the spread of uncertainty which results from using the "pessimistic" and "optimistic" values from Figure 4. These detail calculations are not shown, since they were computed in a manner identical to that shown in Tables 3 and 4.

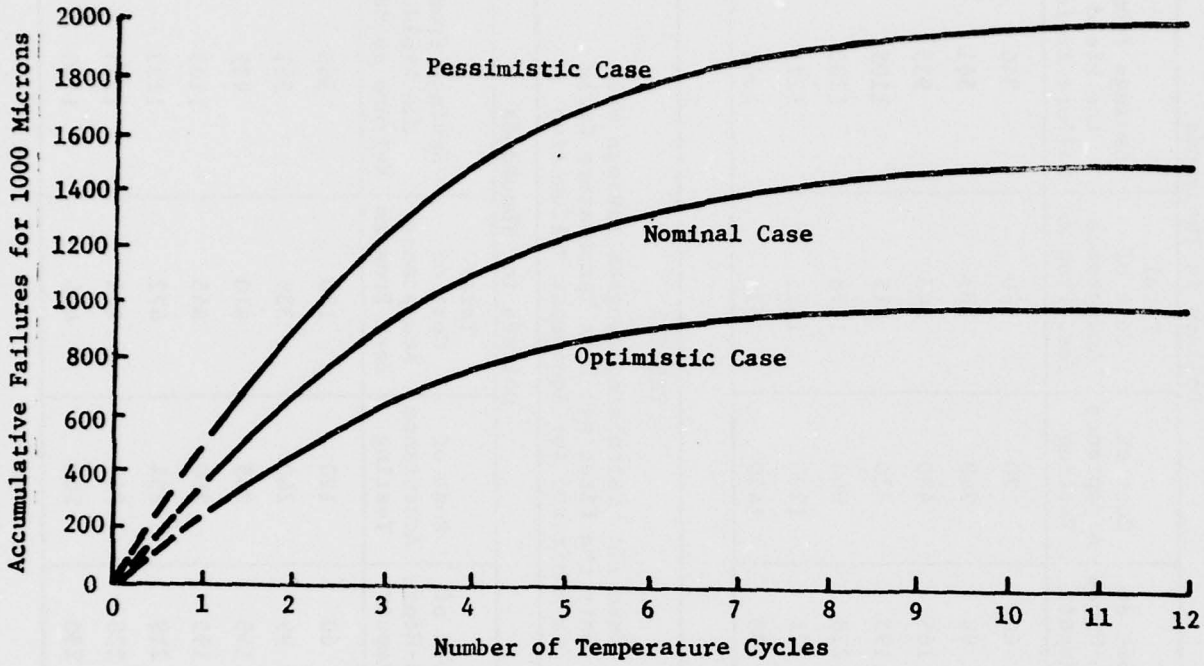

Figure 4 Predicted Acceptance Test Failures for 1000 Microns, As a Function of the Number of Temperature Cycles

TABLE 3

Case I: Calculated Program Savings When Every Temperature Cycle is Monitored for Equipment Malfunction

No. of Temp. Cycles	Acceptance Test Failures in 1000 MICRONS	Dollars in Thousands				
		Cost of In-House Repair	Cost of Acceptance Testing	Total Cost of Acceptance Test Program	Savings from the Field Failure Avoided	Program Savings
1	400	60	120	180	340	160
2	660	99	240	339	561	222
4	1100	165	480	645	935	290
6	1300	195	720	915	1105	190
8	1450	218	960	1178	1233	55
10	1500	225	1200	1425	1275	(150)*
12	1530	230	1440	1670	1301	(369)*

* A loss

TABLE 4

Case II: Calculated Program Savings When Only the First and Last Temperature Cycle is Monitored for Equipment Malfunction

No. of Temp. Cycles	Acceptance Test Failures in 1000 MICRONS	Dollars in Thousands				
		Cost of In-House Repair	Cost of Acceptance Testing	Total Cost of Acceptance Test Program	Savings from the Field Failure Avoided	Program Savings
1	400	60	120	180	340	160
2	660	99	240	339	561	222
4	1100	165	245	410	935	525
6	1300	195	250	445	1105	660
8	1450	218	254	472	1233	761
10	1500	225	259	484	1275	791
12	1530	230	264	494	1300	807

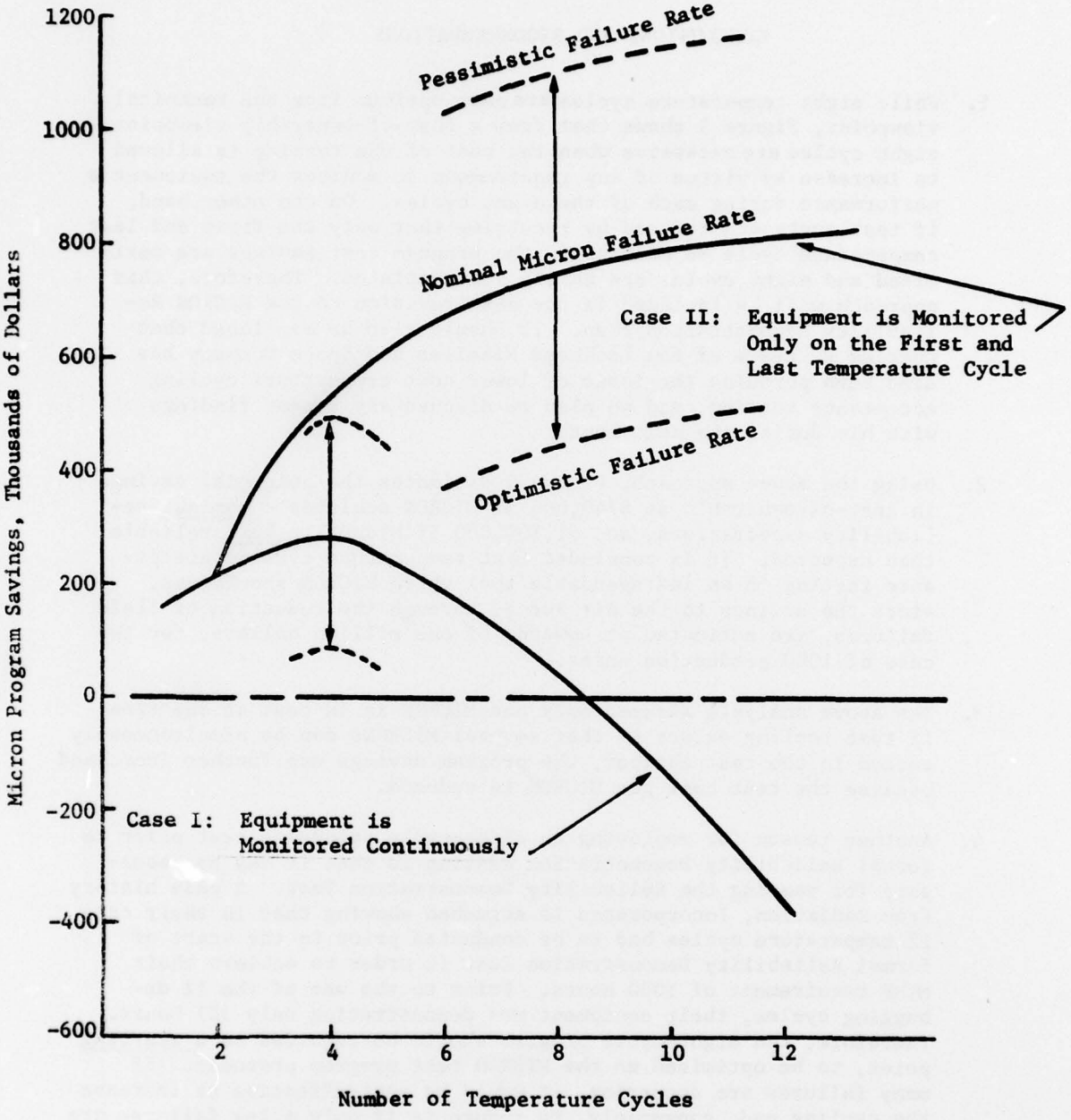

Figure 5 Micron Program Savings vs Number of Temperature Cycles and Frequency of Monitoring

CONCLUSIONS AND RECOMMENDATIONS

1. While eight temperature cycles are near optimum from the technical viewpoint, Figure 5 shows that from a cost-of-ownership viewpoint, eight cycles are excessive when the cost of the testing is allowed to increase by virtue of any requirement to monitor the equipment's performance during each of the eight cycles. On the other hand, if test costs are reduced by requiring that only the first and last temperature cycle be monitored, the program cost savings are maximized and eight cycles are easily substantiated. Therefore, this approach will be included in the next revision to the MICRON Reliability Demonstration Plan. It should also be mentioned that Charles E. Leake of the Lockheed Missiles and Space Company has also been pursuing the issue of lower cost temperature cycling acceptance testing, and we plan to discuss any recent findings with him during the next month.

2. Using the above approach, Figure 5 estimates the potential savings in cost-of-ownership at $740,000 if MICRON achieves a nominal reliability expectations, and $1,100,000 if MICRON is less reliable than expected. It is concluded that temperature cycling acceptance testing is an indispensable tool which MICRON should use, since the savings to the Air Force, through the reduction of field failures, are estimated at upwards of one million dollars, for the case of 1000 production units.

3. The above analysis assumed only one MICRON is in test at one time. If test tooling exists so that several MICRONs can be simultaneously tested in the test chamber, the program savings are further increased because the test cost per MICRON is reduced.

4. Another reason for employing an eight-cycle debugging test prior to formal Reliability Demonstration testing is that it may be necessary for passing the Reliability Demonstration Test. A case history from Radiation, Incorporated is attached showing that in their case 12 temperature cycles had to be conducted prior to the start of formal Reliability Demonstration Test in order to achieve their MTBF requirement of 1000 hours. Prior to the use of the 12 debugging cycles, their equipment was demonstrating only 327 hours. Therefore, the eight-cycle program should be regarded as a starting point, to be optimized as the MICRON test program proceeds. If many failures are occurring, it would be cost-effective to increase the cycling and, conversely, to reduce it if only a few failures are being experienced. This decision should be made using a Cost-of-Ownership Tradeoff Study when failure rate data is obtained from the early acceptance testing.

CASE HISTORY: RADIATION INCORPORATED'S AN/ASW-25

Radiation's experience on the AN/AWS-25 Digital Data Communications Set is an interesting case history. This equipment is the essential data link in the Navy All-Weather Carrier Landing system and has a reliability requirement of a minimum 1000-hour MTBF (one failure or less in 1000 hours of testing). Contractual requirements dictated that all systems be tested for 100 hours (16 cycles) of formal demonstration in the environment of Test Level E of MIL-STD-781. The results of such testing on each month's production constituted a single test in which the minimum requirements were to be demonstrated.

The initial approach was to conduct a "manufacturing run-in test" (MRIT) of up to 24 hours at bench ambient conditions prior to submitting the units to the formal demonstration tests. Early in the program, tests on 234 systems demonstrated an MTBF of 259 hours. Part failure rates in these early demonstrations were considerably higher than those predicted using MIL-HDBK-217A, and the first step toward reliability improvement was to replace I.C.'s having gold-to-aluminum bonding systems. MRIT was also increased to 75 hours. Subsequent tests on equipments with these improvements resulted in an MTBF of 327 hours.

At this point it was noted that the initial test systems demonstrated a much higher reliability when failures from the first reliability tests were repaired and the units retested. Limited data from some of these systems resulted in an MTBF in excess of 1200 hours. As a result, a preconditioning program of a minimum of 75 hours (12 cycles) of Test Level E testing was instituted on all equipments, and the MTBF of several subsequent demonstrations continued to exceed 1200 hours. It was theorized that extending the preconditioning period would lead to further demonstrated reliability improvement by eliminating additional "infant mortality" failures. This was confirmed by demonstration testing of systems with a minimum of 100 hours (16 cycles) of preconditioning, and by further tests after 200 hours (32 cycles) of preconditioning. Initial tests under these conditions demonstrated MTBF's in excess of 1500 and 1700 hours respectively. At the present time, the 200-hour preconditioning period has been adopted as a standard, and systems having this testing have subsequently demonstrated a cumulative MTBF of 1692 during 140,671 unit-hours of testing. The cumulative MTBF of all systems since the 75-hour preconditioning began is 1527 hours during 209,644 unit-hours of testing.

A curve to show the approximate average MTBF as a function of the number of cycles of preconditioning prior to demonstration is shown in Figure 6.

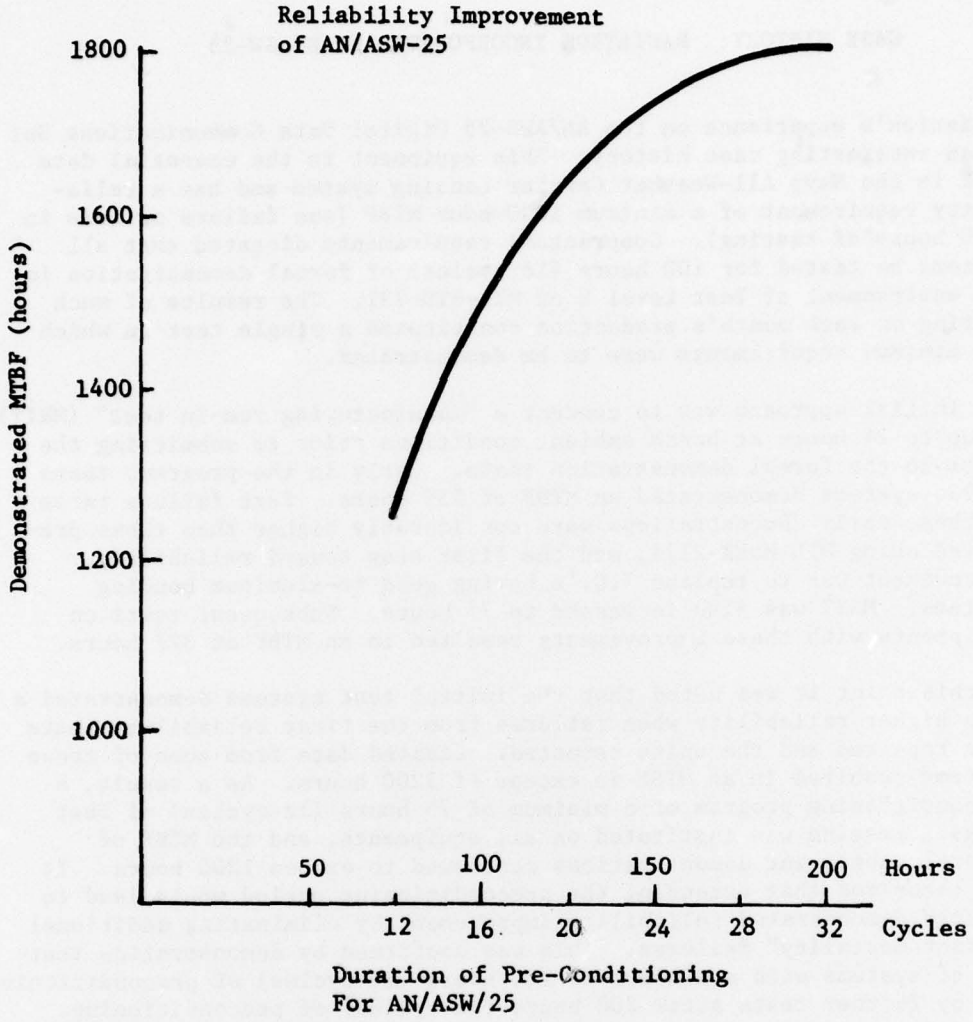

Figure 6 Radiation Incorporated - Temperature Cycling vs Reliability Improvement

APPENDIX H

MEMORANDUM CONCERNING VACUUM PROBLEMS ON MICRON PROGRAM

COPY

MEMORANDUM

Date: March 10, 1975

To: Richard Burrows

From: L. E. Bergquist

Subject: Visit to Autonetics on Vacuum Problems on MICRON Program

cc: J. Martin, S. Russak

On March 3, 4, 5, I was at Autonetics in Anaheim, California consulting on the MICRON program for which Martin has the reliability contract. The heart of the MICRON program is a small ball gyroscope which is enclosed in an evacuated cell. The ball when operating rotates at 2412 hertz and should not change its rotational speed by more than 2 hertz in one year. A small change in pressure can cause this change. The maximum allowable pressure is unknown but expected to be in the 10^{-7} torr region. To keep this cell evacuated, two types of pump are being studies. One is a small ion pump, the other a zirconium graphite getter that is made by S.A.E.S. in Milan, Italy. The getter is preferred if a sealed assembly can be achieved because no power supply is needed once the getter is activated. The getter is activated in the final process of assembling the unit. However, the getter does not pump noble gases so the seals on the gyroscope must be extremely leak free with leakage rates below 10^{-12} Atm-cc/sec of helium. Presently, several ceramic metal electrical feedthroughs are required for the gyro operation. Ceramaseal supplies these feedthroughs and their leak rates are guaranteed to be less than 1×10^{-9} Atm-cc/sec of helium. If this is a molecular leak and the internal volume is 3/4 $inch^3$ in the gyro, an internal pressure of 5×10^{-6} torr helium will result in one year and a pressure of 3.119×10^{-3} torr of Argon in one year. This assumes that the gyro is stored at standard temperature conditions. Seals must have leak rates much less than 10^{-12} Atm-cc/sec of helium if one expects any long-term reliability. This may require new developments in ceramic feedthroughs. If leak rates of 10^{-12} are achieved, the leakage will likely be by difussion through the material and only helium will enter. Argon is too large a molecule. However, these seals will need to be tested. The only known leak detector that can detect leaks this small is the one in our laboratory at Martin.

Problems discussed and followed up on were:

1. They have had difficulty in starting the ion pump once it has been evacuated. They desire to have it start in a few seconds and it has taken as long as 30 minutes for it to start once the gyro is evacuated. In a previous communication, I suggested putting a

filament in the system which could be heated by a small voltage and outgas enough to raise the pressure enough so the pump would start quickly. The method has been tried and the pump starts in a few seconds. They are now planning to incorporate a 97% tungsten 3% rhenium filament into this system.

2. Seals used in assembling the gyro have leaked. Indium was tried, but it has a melting point of 154°C which is too low for the required bakeout and also leaked when the getter was activated. Gold wire was tried, but they were crossing the ends of the wire rather than bonding them. This required extra force at the overlapping joint and the seal leaked. I suggest they buy bonded gold wire seals from a manufacturer such as Western Gold and Platinum. They will contact them for price and delivery.

3. Vacuum processing of the gyro was discussed and I pointed out that a vacuum bakeout of at least 150°C is necessary to remove the water vapor. Once this temperature is achieved and held during the evacuation cycle a major portion of the water will be released from the surfaces and exhausted. This procedure was tried while I was there and the pressure rose and then dropped rapidly after achieving this temperature.

4. Another area discussed was the entrapment of gases in threads within the gyro. These all need to be slotted so that the gas can escape rapidly.

5. Autonetics has purchased and has in operation an excellent quadrupole and data handling system for use in studying the gases released in vacuum processing the gyro. It can also be useful in studying and obtaining a better understanding of the getter, both during activation and while exhausting the gyro. This system should greatly assist them in improving the relaiblity of the gyro.

/S/ Lyle E. Bergquist
L. E. Bergquist
Payloads, Sensors & Instruments
Section 0560

LEB:dw

Information from Al Gross - April 21, 1975

Subject: Contribution of Lyle Bergquist to Gettered ESG

We found Mr. Bergquist quite helpful when he visited Autonetics in March 1975. We intend to implement his suggestion that calibrated "leaks" are readily made with "partially pinched" copper pinch-off tubes. His advice on the outgassing of water vapor at or above 250°F was also quite valuable, since we had assumed a lower temperature would have been effective. Another important comment was that the elevated temperature baking of the assembled device under vacuum was more important than many of the preceding cleaning operations. In addition, Mr. Bergquist confirmed that we had made correct choices in a myriad of other areas and we found these confirmations fully as important and valuable as those things we hadn't thought of ourselves.

We contemplate requesting services of Mr. Bergquist again for the following purposes:

1. Consultation on changes in techniques or approach.

2. Performance of high resolution leak detection on our hardware at the Denver site.

APPENDIX I

COMMUNICATION REGARDING INITIATION OF FAILURE REPORTING

Failure Reporting Program for MICRON
Phase 2A Engineering Test Operations

(Copy of letter from L. B. Romine to MICRON project personnel)

Effective July 22, 1974, a program of failure reporting and failure analysis will be implemented for the MICRON Phase 2A engineering test operations. For MICRON Phase 2A, this program will apply to tests conducted in conjunction with the N57A-1, N57A-2, Gyro Subassemblies (GSA's) and Gyro Test Stations.

The implemented program will be selectively less formal than that generally utilized for the development and/or production program. However, the familiar Autonetics forms identified in AOM C-30 series procedures (and included in the attachment to this IL) will be utilized for failure and removal reporting and failure analysis.

In Attachment 1 to this letter, the general requirements of this reporting program are summarized. The requirements have been designed to cause a minimum impact on D/244 responsibilities, while still providing much needed documentation to allow Reliability Engineering to establish and analyze failure trends and/or design/hardware problems which may require corrective action. Those listed are requested to familiarize themselves with the reporting/analysis requirements to assure their effective implementation. The individuals with assigned responsibilities are shown in Attachment 3 to this IL.

It should be noted that Mr. Ray Holtz will assume the responsibility of administering and fulfilling the role of Reliability Engineering as identified within the scope of this reporting program. Mr. Holtz is assigned as the on-site reliablity representative of the Martin Marietta Corporation as associate contractor on the MICRON Program.

/S/ L. B. Romine
Manager
MICRON Engineering

APPENDIX J

MICRON FAILURE REPORTING PROGRAM BULLETIN

COPY OF ROCKWELL INTERNATIONAL AUTONETICS GROUP PROGRAM BULLETIN - MICRON

No.: 3
Page: 1 of 3
Date: October 15, 1976

Subject: Failure Reporting, Failure Analysis and Delinquency Monitoring

SCOPE

This program bulletin is applicable to prototype Inertial Navigation Unit (INU) equipment which is fabricated on Phase 2B contract or discretionary resources. It establishes the requirements for initiating the Form for Removal Reporting (FRR), the Part Feedback Envelope (PFE), the failure Analysis Report (AR), and for delinquency monitoring of FRR and AR data.

REQUIREMENTS

1. FRR Form 851-D-1 shall be utilized for all reportable events of serialized assemblies subsequent to the successful completion of their individual engineering functional tests.

   The definitions and instructions to initiate and closeout the FRR are as defined in AOM C-30.1, except for the four differences listed below:

   a. FRR Blocks which do not require entries are 00, 05, 16, 17, 19, 22, 24, 25, 27, 29, 30, 31, 32 (4), 32 (5) and 32 (6), 34, 35, 37, 43, 44, 45, 47, 51, 54 and 56.

   b. Reliability Engineering will assume the role of the Failure Data Center for monitoring the adequacy of the failure description, and the completion and timely closeout of FRR's.

   c. A Reliability Engineering stamp in Block 50 is sufficient to effect FRR closeout.

   d. For all post-acceptance failures, Block 53 shall be signatured by:

      (1) The engineer responsible for the reportable item design.

      (2) The Reliability Engineer.

2. PFE Forms 851-D-20 shall be initiated and completed in accordance with the FRR and PFE Instruction Manual (S70-1/501), but utilizing only Blocks 02, 05, 06, 08, 09, 13, 14, 15 and 16, for each nonreparable

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REVISED BULLETIN. Supersedes MICRON Program Bulletin No. 3 dated August 30, 1974. Revised to update for Phase 2B.

electronic part or electrical/mechanical component removed from a reparable assembly. This requirement applied to failures and suspected failures which occur subsequent to initial Quality Assurance acceptance of the item.

3. AR Form 851-D-6 shall be initiated and completed in accordance with AOM C-30.2. The AR shall be initiated to document failure trends or critical system failures (such as an ESG rotor drop). The engineer responsible for the design of the failed reportable item shall be responsible for accomplishing the failure analysis and preparation of the AR. Reliability Engineering shall be responsible for reviewing and approving each AR with particular regard for the impact of recommended corrective action on design/hardware reliability requirements. A Failure-Action Review Board will review all AR's where design/hardware corrective action is recommended to resolve the documented problem. As necessary, the AR will be amended to include corrective action recommended by the Review Board to resolve the problem.

4. Failure-Action Review Board: Responsible engineers and their department/group supervision, together with representatives from Reliability, Engineering, Program Management, and the MICRON Project Engineer shall convene as participants on a Failure-Action Review Board. The MICRON Project Engineer, or his delegated representative, shall serve as chairman of the Review Board. Any additional participants, at any given board meeting, will depend on the nature and scope of the problem under investigation (i.e., engineering, manufacturing operations, quality assurance, logistics, etc.).

   The Review Board will convene to consider failure-corrective actions taken or planned for observed failure trends and all critical system failures. The board meetings will not be convened on a scheduled basis, but as often as necessary depending on the number and/or criticality of failure-corrective actions to be reviewed. The recommendations and decisions of the board regarding proposed or completed corrective actions shall be documented in the MICRON Reliability Problem Log.

   A MICRON Reliability Problem Log shall be used to document the reliability problems. The log shall be maintained by Reliability Engineering. As a minimum, the Log shall contain the following information for each documented problem:

   a. Problem Number. Numbers shall be assigned sequentially.

   b. Description of the problem.

   c. Impact on reliability.

d. Status, listed chronologically, of problem investigation, analysis, and any assigned action items.

e. Recommendations and decisions of the Board regarding proposed or completed corrective actions and action effectivity dates.

f. The Board's assessment of corrective action with regard to reliability impact.

5. Failed items requiring hardware analysis may be identified with a Reliability Engineering Analysis (REA) tag (Form 851-F-10) to facilitate control and statusing of these items during evaluation and rework. Reliability Engineering will prepare the REA tag and attach it to the hardware item or associated paper work. The tag will be removed upon completion of the required evaluation and rework, or deletion of the analysis requirement. Evaluation, repair and test of REA-tagged items will be expedited to provide the Responsible Design Engineers with data pertinent to timely analysis and correction of the causes of the failures.

6. Reliability Engineering will assume the role of the Failure Data Center to monitor FRR and AR delinquencies. FRR and AR documents on events other than failures or on events not requiring comprehensive analysis, will not become delinquent. The delinquency criteria will be:

		AR**	
	FRR*	No PMA Required	PMA Required
CPC's	20 days	10 days	20 days
EMA's	20 days	10 days	20 days
ESG's	20 days	10 days	20 days
Modules	10 days	10 days	20 days
Battery	10 days	N/A	N/A
Mechanical Housing Unit	10 days	10 days	N/A
System	30 days	30 days	N/A

* Calendar days from the FRR date of event.
** Calendar days from the date of (a) FRR completion if Autonetics rework or (b) Autonetics receipt of rework or analysis data if supplier rework. AR delinquency criteria is dependent on requirements for Post Mortem Analysis (PMA).

/S/ J. A. Schwarz
MICRON Program Manager
Strategic Systems Division